L4 \textit{eXperimental} Kernel
Reference Manual

Version X.2

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# Contents

## About This Manual
- Introductory Remarks .................................................. v
- Understanding This Document .................................. vi
- Notation ........................................................................ vii
- Using the API ................................................................. viii
- Revision History ............................................................. ix

## 1 Basic Kernel Interface
1.1 Kernel Interface Page .................................................. 2
1.2 KERNELINTERFACE .................................................. 7
1.3 Virtual Registers ......................................................... 11

## 2 Threads
2.1 ThreadId ........................................................................ 14
2.2 Thread Control Registers (TCRs) ................................. 16
2.3 EXCHANGEREGISTERS .............................................. 18
2.4 THREADCONTROL .................................................... 22

## 3 Scheduling
3.1 Clock ........................................................................... 26
3.2 SYSTEMCLOCK .......................................................... 27
3.3 Time ............................................................................ 28
3.4 THREADSWITCH ......................................................... 30
3.5 SCHEDULE ................................................................. 31
3.6 Preempt Flags ............................................................... 34

## 4 Address Spaces and Mapping
4.1 Fpage ........................................................................... 36
4.2 UNMAP ......................................................................... 38
4.3 SPACECONTROL ........................................................ 41

## 5 IPC
5.1 Messages And Message Registers (MRs) ...................... 44
5.2 MapItem ........................................................................ 49
5.3 GrantItem ...................................................................... 51
5.4 StringItem ..................................................................... 52
5.5 String Buffers And Buffer Registers (BRs) ................. 55
5.6 IPC ............................................................................... 57

## 6 Miscellaneous
6.1 ExceptionHandler ........................................................ 66
6.2 Cop Flags ....................................................................... 67
6.3 PROCESSORCONTROL .............................................. 68
6.4 MEMORYCONTROL ..................................................... 70

## 7 Protocols
7.1 Thread Start Protocol .................................................... 74
7.2 Interrupt Protocol ........................................................ 75
7.3 Pagefault Protocol ......................................................... 76
7.4 Preemption Protocol ...................................................... 77
7.5 Exception Protocol ......................................................... 78
7.6 Sigma0 RPC protocol .................................................. 79
7.7 Generic Booting ............................................................. 82
About This Manual

Introductory Remarks

Purpose of This Document
This L4 Reference Manual serves as defining document for all L4 APIs and ABIs. Primarily, it addresses L4 microkernel implementors as API/ABI suppliers and code-generator or library implementors as API/ABI users. The reference manual assumes intimate knowledge of basic L4 concepts and hardware architecture. Its key point is precise definition, not explanation and illustration. The L4 System Programmer’s Manual is intended to support programmers using L4. It explains and illustrates fundamental concepts and describes in more detail how (and why) to use which function, etc.

Maintainers
The document is maintained by the following members of the L4Ka Team:

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Credits
This manual is based on a final draft by Jochen Liedtke. It reflects his outstanding work on the L4 microkernel and systems research in general. Only his vision of system design made this work possible. Jochen defined the state of the art of microkernel design for nearly a decade. We thank him for his support and try to continue the work in his spirit.

Helpful contributions for improving this reference manual and the L4 interface came from many persons, in particular from Alan Au, Marcus Brinkmann, Kevin Elphinstone, Bryan Ford, Andreas Haeberlen, Hermann Härtig, Gernot Heiser, Michael Hohmuth, Trent Jaeger, Jork Löser, Frank Mehrert, Yoonho Park, Marc Salem, Carl van Schaik, Sebastian Schönberg, Cristan Szmajda, Marcus Völp, Neal Walfield, Adam Wiggins, Simon Winwood, and Jean Wolter.

Document History
<table>
<thead>
<tr>
<th>Event</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>draft by Jochen Liedtke</td>
<td>??/?? - 06/01</td>
</tr>
<tr>
<td>review by L4Ka Team</td>
<td>06/01 - 09/01</td>
</tr>
<tr>
<td>L4 developers review</td>
<td>Q4/01</td>
</tr>
<tr>
<td>release</td>
<td>01/02</td>
</tr>
</tbody>
</table>
Understanding This Document

This L4 Reference Manual defines the generic API for all 32-bit and 64-bit machines. As such, the generic reference manual is independent of specific processor architectures. It is complemented by processor-specific ABI specifications. Some of them can be found in the appendix of this document.

In this document, we differentiate between Logical Interface, Generic Binary Interface, Generic Programming Interface, Convenience Programming Interface and Processor-specific Binary Interface.

**Logical Interface**
The logical interface defines all concepts and logical objects such as system-call operations, logical data objects, data types and their semantics. Altogether, they form the logical L4 API.

**Generic Binary Interface**
Binary representations of most data types and generic data objects are defined independently of specific processors (although there are two different versions, one for 32-bit and a second one for 64-bit processors). Both versions together form the generic binary interface of L4.

From a purist point of view, logical interface plus generic binary interface could be regarded as a complete specification of the hardware-independent L4 microkernel interface. However, for ease-of-use and standardization reasons, the mentioned two fundamental interfaces are complemented by two more interface classes:

**Generic Programming Interface**
The generic programming interface defines the objects of the logical interface and the generic binary interface as pseudo C++ classes. The language bindings for regular C is for the most part identical to C++. For the cases where the C language causes function naming conflicts, the C version of the function name is given in brackets.

For the time being, only the C and C++ versions of the API are specified. The concrete syntax of other language interfaces will be left open. Later on, all language bindings will be included in the generic programming interface.

**Convenience Programming Interface**
This interface is not part of the L4 microkernel specification in the strict sense. All of its data types and procedures can be implemented using the generic programming interface. Strictly speaking, it is an interface on top of the microkernel that makes the most common operations more easily usable for the programmer.

It is important to understand that convenience and ease-of-use, not completeness, is the criterion for this interface. The convenience programming interface supports programmers by offering operations that together cover about 95% of the required microkernel functionality. For the remaining 5%, the programmer has to use the basic (not so convenient) operations of the generic programming interface.

Obviously, the convenience programming interface is not mandatory. Consequently, from a minimalist point of view, there is no need to include it in the generic L4 specification.

*Nevertheless, for reasons of standardization and thus portability of software, every complete L4 language binding has to include the entire convenience programming interface.*

Implementation remark: Although the convenience interface can be completely implemented on top of the generic programming interface, i.e., processor independently, the implementor of the convenience interface may implement it hardware-dependently and thus incorporate any optimization that becomes possible through a specific processor-specific binary interface.

The last interface class is not part of the generic L4 API specification.

**Processor-specific Binary Interface**
Defines the processor-specific binary interface.
Notation

Basic Data Types
This reference manual describes the L4 API and ABI for both 32-bit and 64-bit processors. The data type Word denotes a 32-bit unsigned integer on a 32-bit processor and a 64-bit unsigned integer on a 64-bit processor. Word64, Word32, and Word16 denote 64, 32, and 16-bit words independent of the processor type.

Privileged Threads
Some system calls can only be executed by privileged threads. Any thread belonging to the same address space as one of the initial threads created by the kernel upon boot-time (see page 82) are treated as privileged.

Bit Fields
Bit-field lengths are denoted as subscripts \((i/j)\) where \(i\) relates to a 32-bit processor and \(j\) to a 64-bit processor. Bit-field subscripts \((i)\) specify bit fields that have the same size for both 32-bit and 64-bit processors. Byte offsets are given as \(\pm i / \pm j\) for 32-bit and 64-bit processors. If all bit-fields of a specified word only adds up to 32 bits, the remaining upper 32 bits on 64-bit processors are undefined or ignored.

Undefined, Ignored, and Unchanged

\(\sim\) Output parameters or bit fields can be undefined. Corresponding parameters or fields are denoted by \(\sim\). They have no defined value on output, i.e., they may have any value or may even be unaccessible. Any algorithm relying on the value of undefined parameters or bit fields is defined to be incorrect.

\(-\) Input parameters or bit fields can be specified as ignored, denoted by \(-\). Such parameters or fields can hold any value without affecting the invoked service. \(-\) is also used to define bit fields that are available for additional information. For example, fpage denotations contain some ignored bits that are used for access control bits in some system calls.

\(\equiv\) In processor-specific interfaces, registers are sometimes defined to be unchanged. This is denoted by \(\equiv\).

Upward Compatibility
The following holds for future API versions and sub-versions that are specified as upward-compatible to the current version.

Output parameters and bit fields.
Fields currently defined as undefined \((\sim)\) may be specified as defined. Such newly defined fields will only deliver additional information. They can be ignored if the system call is used exactly like specified in the current API.

Input parameters and bit fields.
Fields currently defined as ignored \((-\) may be specified as defined. However, the content of such fields will be only relevant for newly defined features. Such fields will be ignored if a system call is used with the “old” semantics specified in this API.
Using the API

Naming
A programmer can use all function, type, and constant definitions defined in the generic and convenience programming interfaces throughout this manual. All definitions must, however, be prefixed with the string “L4_” and type names must contain the “_t” suffix (e.g., use “L4_Ipc ()” and “L4_MsgTag_t” rather than “Ipc ()” and “MsgTag”). The interfaces are currently only defined for C++ and C. In some cases the naming used for function names causes conflicts in the C language. These conflicts must be resolved using the alternative name specified in brackets after the function definition.

Include Files
The relevant include files containing the required definitions and declarations are specified in the beginning of the generic and convenience interface sections. In general there is one include file for each chapter in the manual. If only the basic L4 data types are needed they can be included using <l4/types.h>.
Revision History

Revision 1
Initial revision.

Revision 2
- Clarified the specification of the kernel-interface page and kernel configuration page magic.
- UntypedWords and StringItems Acceptor constants collided with function UntypedWords(MsgTag) and StringItems(MsgTag) function declaration. Renamed to UntypedWordsAcceptor and StringItemsAcceptor.
- Changed kernel ids for L4Ka kernels.
- Fixed return types for operators on the Time type.
- Changed wrx access rights in fpages to rwx. Also changed WRX reference bits in fpages returned from UNMAP system call to RWX.
- Renamed Put functions operating on MsgBuffer to Append.
- Address space deletion is now performed by deleting the last thread of an AS. This makes creation and deletion symmetrical (via ThreadControl). Before, all threads but the last were deleted by ThreadControl, and the last by SpaceControl.
- Added functions for creating ThreadIDs and for retrieving version and thread numbers from them. Fixed size of MyLocalId and MyGlobalId TCRs.
- Specified that the first three thread version numbers available for user threads are dedicated to $\sigma_0$, $\sigma_1$, and root task respectively.
- Changed the encoding of $\mu$ in the magic field of the KIP back to 0xE6 to be compatible with previous versions of the kernel.
- Changed memory descriptors (e.g., dedicated memory) in the kernel-interface page and kernel configuration page to use an array of typed descriptors instead of a static number of predefined ones.
- Added an appendix for the PowerPC interface.
- Added Niltag MsgTag constant.
- Decreased size of MsgBuffer structure to 32.
- Changed single Fpage& argument of Unmap() and Flush() into pass by value.
- Changed the ia32 kernel feature string “small” to “smallspaces”.
- Added appendix for the ia64 interface.
- Changed the ia32 IPC and LIPC ABI to be better suitable for common hardware featuring sysenter/sysexit and gcc.
- Added ProcDesc convenience functions.
- Specified which include files to use for the various parts of the API.
- Allow privileged threads to access ia32 Model-Specific Registers.
- Changed the ia64 ABI for system-call links and the IPC and LIPC system-calls.
- The UTCB location of a new thread is now explicitly specified by a parameter to the THREADCONTROL system-call.
- Added C versions of conflicting function names.
- Added a number of convenience functions for fpages, map items, grant items, string items and kernel interface page fields.
- Added description of the send base in map and grant items.
- Changed subversion numbering for Version X.2 and Version 4 API.
- Renamed the XferTimeout TCR to XferTimeouts and split into separate send and receive timeouts.
- Added two thread specific words to each the architecture specific TCR sections. These words are free to be used by, e.g., IDL compilers.
- Changed name of L4Ka kernels to the official name. Added L4Ka::Strawberry.
- Added appendices for Alpha and MIPS64.

Revision 3
- Clarified description of the supplier field in the kernel-interface page.
- Added NumMemoryDescriptors() convenience function.
- Clarified the return value of MemoryDescType() function.
- Fixed faulty specification of Wait_Timeout() and ReplyWait_Timeout().
- Added a new h-flag to control parameter in the EXCHANGEREGISTERS system-call. The h-flag controls whether the resume/halt flag should be ignored or not.
- Changed parameter type of TimePeriod() from “int” to “Word64”.
- Fixed typo in specification of the MsgTag input/output IPC parameter.
- Added comment to IPC system-call about the read-once semantics of message registers.
- Added member name “raw” to all L4 types declared as structs.
- Renamed start() and stop() functions to Start() and Stop().
- Describe semantics of undefined UTCB memory regions.
- The first 10 message registers on PowerPC are now defined as backed by physical registers.
- The first 9 message registers on Alpha are now defined as backed by physical registers.
- Fixed MR_0 register allocation for IA32 syscalls and adapted syscalls accordingly.

Revision 4
- Added appendix for AMD64.
- Changed MIPS64 IPC ABI to include 9 message registers.
- Added SYSTEMCLOCK syscall for MIPS64.
- Clarified the fact that an interrupt thread may be the originator thread during IPC propagation.
- Added appendix for SPARC v9.
- The high field of memory descriptors now specify the last addressable byte in the memory region.
Chapter 1

Basic Kernel Interface
1.1 Kernel Interface Page  [Data Structure]

The kernel-interface page contains API and kernel version data, system descriptors including memory descriptors, and system-call links. The remainder of the page is undefined.

The page is a microkernel object. It is directly mapped through the microkernel into each address space upon address-space creation. It is not mapped by a pager, can not be mapped or granted to another address space and can not be unmapped. The creator of a new address space can specify the address where the kernel interface page has to be mapped. This address will remain constant through the lifetime of that address space. Any thread can obtain the address of the kernel interface page through the KERNEL_INTERFACE system call (see page 7).

<table>
<thead>
<tr>
<th>L4 version parts</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supplier</td>
</tr>
<tr>
<td>~</td>
</tr>
<tr>
<td>~</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SCHEDULE SC</th>
<th>THREADSWITCH SC</th>
<th>SYSTEMCLOCK SC</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXCHANGEREGISTERS pSC</td>
<td>UNMAP pSC</td>
<td>LPC pSC</td>
</tr>
<tr>
<td>+F0 / +1E0</td>
<td>+E0 / +1C0</td>
<td>+D0 / +1A0</td>
</tr>
<tr>
<td>MEMORYCONTROL pSC</td>
<td>PROCESSORCONTROL pSC</td>
<td>THREADCONTROL pSC</td>
</tr>
<tr>
<td>ProcessorInfo</td>
<td>PagingInfo</td>
<td>ThreadInfo</td>
</tr>
<tr>
<td>+C0 / +180</td>
<td>+B0 / +160</td>
<td>+A0 / +140</td>
</tr>
<tr>
<td>~</td>
<td>~</td>
<td>~</td>
</tr>
<tr>
<td>~</td>
<td>~</td>
<td>~</td>
</tr>
<tr>
<td>~</td>
<td>~</td>
<td>~</td>
</tr>
<tr>
<td>~</td>
<td>MemoryInfo</td>
<td>~</td>
</tr>
<tr>
<td>~</td>
<td>~</td>
<td>~</td>
</tr>
<tr>
<td>~</td>
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<td>~</td>
</tr>
<tr>
<td>~</td>
<td>~</td>
<td>~</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>KernDescPtr</th>
<th>API Flags</th>
<th>API Version</th>
<th>~ (0/32)</th>
<th>K</th>
<th>E</th>
<th>D</th>
<th>L</th>
</tr>
</thead>
<tbody>
<tr>
<td>+C / +18</td>
<td>+8 / +10</td>
<td>+4 / +8</td>
<td>+0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Note that this kernel interface page is basically upward compatible to the kernel info page of versions 2 and X.0. Only the former clock field is missing and now used differently. The magic byte string “L4µK” at the beginning of the object identifies the kernel interface page.

**Version/id number convention:** Version/subversion/subsubversion numbers and id/subid numbers with the most significant bit 0 denote official versions/ids and are globally unique through all suppliers. Version/id numbers that have the most significant bit set to 1 denote experimental versions/ids and may be unique only in the context of a supplier.

## API Description

<table>
<thead>
<tr>
<th>API Version</th>
<th>version (8)</th>
<th>subversion (8)</th>
<th>~ (16)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x02</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x83 0x80</td>
<td>Version 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x83 0x81</td>
<td>Experimental Version X.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x84 rev</td>
<td>Experimental Version X.2 (Revision rev)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x04 rev</td>
<td>Version 4 (Revision rev)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>API Flags</th>
<th>~ (28/60)</th>
<th>ee</th>
<th>wu</th>
</tr>
</thead>
<tbody>
<tr>
<td>ee</td>
<td>= 00: little endian, = 01: big endian.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>wu</td>
<td>= 00: 32-bit API, = 01: 64-bit API.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note that this field can not be used directly to differentiate between little endian and big endian mode since the ee field resides in different bytes for both modes. Furthermore, the offset address of the API Flags is different for 32-bit and 64-bit modes. In summary, a direct inspection of the kernel interface page is not sufficient to securely differentiate between 32/64-bit modes and little/big endian modes.

Secure mode detection is enabled through the `KERNELINTERFACE` system call (see page 7). It delivers the API Flags in a register.

## System Description

<table>
<thead>
<tr>
<th>ProcessorInfo</th>
<th>8 (4)</th>
<th>~ (12/44)</th>
<th>processors − 1 (16)</th>
</tr>
</thead>
<tbody>
<tr>
<td>s</td>
<td>The size of the area occupied by a single processor description is $2^s$. Location of description fields for the first processor is denoted by <code>ProcDescPtr</code>. Description fields for subsequent processors are located directly following the previous one.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>processors</td>
<td>Number of available system processors.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PageInfo</th>
<th>page-size mask (22/54)</th>
<th>~ (7)</th>
<th>r w x</th>
</tr>
</thead>
<tbody>
<tr>
<td>page-size mask</td>
<td>If bit $k$ of the page-size mask field (bit $k$ of the entire word) is set to 1 hardware and kernel support pages of size $2^k$. If the bit is 0 hardware and/or kernel do not support pages of size $2^k$. Note that pages of size $2^k$ can be used, even if $2^k$ is no supported hardware page size. Information about supported hardware page sizes is only a performance hint.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Identifies the supported access rights (read, write, execute) that can be set independently of other access rights. A 1-bit signals that the right can be set and reset on a mapped page. For $rwx = 010$, only write permission could be controlled orthogonally. The processor would implicitly permit read and execute access on any mapped page. For $rwx = 111$, all three rights could be set and reset independently.

**ThreadInfo**

<table>
<thead>
<tr>
<th>UserBase (12)</th>
<th>SystemBase (12)</th>
<th>t (8)</th>
</tr>
</thead>
</table>

$t$ Number of valid thread-number bits. The thread number field may be larger but only bits $0 \ldots t-1$ are significant for this kernel. Higher bits must all be 0.

**UserBase**

Lowest thread number available for user threads (see page 14). The first three thread numbers will be used for the initial thread of $\sigma_0, \sigma_1$, and root task respectively (see page 82). The version numbers (see page 14) for these initial threads will equal to one.

**SystemBase**

Lowest thread number used for system threads (see page 14). Thread numbers below this value denote hardware interrupts.

**ClockInfo**

<table>
<thead>
<tr>
<th>SchedulePrecision (16)</th>
<th>ReadPrecision (16)</th>
</tr>
</thead>
</table>

**ReadPrecision**

Specifies the minimal time difference $\neq 0$ that can be detected by reading the system clock through the `SYSTEMCLOCK` system call. Basically, this is the precision of the system clock when reading it.

**SchedulePrecision**

Specifies the maximal jitter ($\pm$) for a scheduled thread activation based on a wakeup time (provided that no thread of higher or equal priority is active and timer interrupts are enabled). Precisions are given as time periods (see page 28).

**UtcbInfo**

<table>
<thead>
<tr>
<th>$s$ (6)</th>
<th>$a$ (6)</th>
<th>$m$ (10)</th>
</tr>
</thead>
</table>

$s$ The minimal area size for an address space’s UTCB area is $2^s$. The size of the UTCB area limits the total number of threads $k$ to $2^s mk \leq 2^s$.

$m$ UTCB size multiplier.

$a$ The UTCB location must be aligned to $2^a$. The total size required for one UTCB is $2^a m$.

**KipAreaInfo**

<table>
<thead>
<tr>
<th>$s$ (6)</th>
</tr>
</thead>
</table>

$s$ The size of the kernel interface page area is $2^s$.

**BootInfo**

Prior to kernel initialization a boot loader can write an arbitrary value into the BootInfo field of the kernel configuration page (see page 82). Post-initialization code, e.g., a root server can later read the field from the kernel interface page. Its value is neither changed nor interpreted by the kernel. This is a generic method for passing system information across kernel initialization.

### Processor Description

**ProcDescPtr**

Points to an array containing a description for each system processor. The `ProcessorInfo` field contains the dimension of the array. `ProcDescPtr` is given as an address relative to the kernel interface page’s base address.

**ExternalFreq**

External Bus frequency in kHz.
**InternalFreq**

Internal processor frequency in kHz.

---

**Kernel Description**

**KernDescPtr**

Points to a region that contains 4 kernel-version words (see below) followed by a number of 0-terminated plaintext strings. The first plaintext string identifies the current kernel followed by further optional kernel-specific versioning information. The remaining plaintext strings identify architecture dependent kernel features (see Appendix A.3). A zero length string (i.e., a string containing only a 0-character) terminates the list of feature descriptions. KernelDescPtr is given as an address relative to the kernel interface page’s base address.

**KernelId**

Can be used to identify the microkernel.

<table>
<thead>
<tr>
<th>id</th>
<th>subid</th>
<th>kernel</th>
<th>supplier</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>L4/486</td>
<td>GMD</td>
</tr>
<tr>
<td>0</td>
<td>2</td>
<td>L4/Pentium</td>
<td>IBM</td>
</tr>
<tr>
<td>0</td>
<td>3</td>
<td>L4/x86</td>
<td>UKa</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>L4/Mips</td>
<td>UNSW</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>L4/Alpha</td>
<td>TUD, UNSW</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>Fiasco</td>
<td>TUD</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>L4Ka::Hazelnut</td>
<td>UKa</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>L4Ka::Pistachio</td>
<td>UKa</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
<td>L4Ka::Strawberry</td>
<td>UKa</td>
</tr>
</tbody>
</table>

**KernelGenDate**

Kernel generation date.

**KernelVer**

Can be used to identify the microkernel version. Note that this kernel version is not necessarily related to the API version.

**Supplier**

The four least significant bytes of the supplier field specify a character string identifying the kernel supplier:

- “GMD”
- “IBM”
- “UNSW”
- “TUD”
- “UKa”

**System-Call Links**

**SC**

Link for normal system call.

**pSC**

Link for privileged system call, i.e., a system call that can only be performed by a privileged thread.

The system-call links specify how the application can invoke system-calls for the current microkernel. The interpretation of the system-call links is ABI specific, but will typically be addresses relative to the kernel interface page’s base address where kernel provided system-call stubs are located.
Memory Description

MemoryInfo

MemDescPtr (16/32) n (16/32)

MemDescPtr
Location of first memory descriptor (as an offset relative to the kernel-interface page’s base address). Subsequent memory descriptors are located directly following the first one. For memory descriptors that specify overlapping memory regions, later descriptors take precedence over earlier ones.

n
Number of memory descriptors.

MemoryDesc

\[
\begin{array}{c|c|c|c}
\text{high}/2^{10} & \sim (10) & +4/+8 \\
\hline
\text{low}/2^{10} & v & t(4) & \text{type}(4) & +0 \\
\end{array}
\]

\text{high}
Address of last byte in memory region. The ten least significant address bits are all hardwired to 1.

\text{low}
Address of first byte in memory region. The ten least significant address bits are all hardwired to 0.

\(v\)
Indicates whether memory descriptor refers to physical memory \((v = 0)\) or virtual memory \((v = 1)\).

\(\text{type}\)
Identifies the type of the memory descriptor.

<table>
<thead>
<tr>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Undefined</td>
</tr>
<tr>
<td>0x1</td>
<td>Conventional memory</td>
</tr>
<tr>
<td>0x2</td>
<td>Reserved memory (i.e., reserved by kernel)</td>
</tr>
<tr>
<td>0x3</td>
<td>Dedicated memory (i.e., memory not available to user)</td>
</tr>
<tr>
<td>0x4</td>
<td>Shared memory (i.e., available to all users)</td>
</tr>
<tr>
<td>0xE</td>
<td>Defined by boot loader</td>
</tr>
<tr>
<td>0xF</td>
<td>Architecture dependent</td>
</tr>
</tbody>
</table>

\(t, \text{ type} = 0xE\)
The type of the memory descriptor is dependent on the bootloader. The \(t\) field specifies the exact semantics. Refer to boot loader specification for more info.

\(t, \text{ type} = 0xF\)
The type of the memory descriptor is architecture dependent. The \(t\) field specifies the exact semantics. Refer to architecture specific part for more info (see page 113).

\(t, \text{ type} \neq 0xE, \text{ type} \neq 0xF\)
The type of the memory descriptor is solely defined by the type field. The content of the \(t\) field is undefined.
1.2 **KERNELINTERFACE**  [Slow Systemcall]

Delivers base address of the *kernel interface page*, *API version*, and *API flags*. The latter two values are copies of the corresponding fields in the kernel interface page. The API information is delivered in registers through this system call (a) to enable unrestricted structural changes of the kernel interface page in future versions, and (b) to enable secure detection of the kernel’s endian mode (little/big) and word width (32/64).

The structure of the *kernel interface page* is described on page 2. The page is a microkernel object. It is directly mapped through the microkernel into each address space upon address-space creation. It is *not* mapped by a pager, can not be mapped or granted to another address space and can *not* be unmapped. The creator of a new address space can specify the address where the kernel interface page has to be mapped. This address will remain constant through the lifetime of that address space.

Any thread can determine the address of the kernel interface page through this system call. Since the system call may be slow it is highly recommended to store the address in a static variable for further use.

It is also possible to use a unique address for the kernel interface page in all address spaces of a (sub)system. Then, the kernel interface page can be accessed by fixed absolute addresses without using the current system call.

Besides other things, the page describes the current API, ABI, and microkernel version so that a server or an application can find out whether and how it can run on the current microkernel. Since the kernel interface page also contains API- and ABI-specific data for most other system calls the page’s base address is typically required before any other system call can be used.

To enable version detection independently of the API and ABI, the current system call is guaranteed to work in all L4 versions. The systemcall code will never change and will be the same on compatible processors. (If a processor is upward compatible to multiple incompatible processors the kernel should offer multiple systemcall codes for this function.)

### Output Parameters

**kernel interface page**

**Ver X.1 and above**

<table>
<thead>
<tr>
<th>base address</th>
<th>(32/64)</th>
</tr>
</thead>
</table>

Kernel interface page address, always page aligned. 0 is no valid address.

**Ver X.0 and below**

| 0 | (32/64) |

Older versions (2, X.0, etc.) do not include the kernel interface page as a kernel mapped page. No address is delivered.

**API Version**

| version (8) | subversion (8) | ~ (16) |

see page 3, “Kernel Interface Page”

**API Flags**

| ~ (28/60) | wee |

see page 3, “Kernel Interface Page”
KernelId

| id (8) | subid (8) | ~ (16) |

see page 5, “Kernel Interface Page”

Pagefaults

No pagefaults will happen.

Generic Programming Interface

System-Call Function:

#include <l4/kip.h>

Void * KernelInterface (Word & ApiVersion, ApiFlags, KernelId)

Convenience Programming Interface

Derived Functions:

#include <l4/kip.h>

struct MEMORYDESC { Word raw[2] }

struct PROCDESC { Word raw[4] }

Void* KernelInterface () [GetKernelInterface]

Delivers a pointer to the kernel interface page.

Word ApiVersion ()

Word ApiFlags ()

Word KernelId ()

Void KernelGenDate (Void* KernelInterface, Word & year, month, day)

Word KernelVersion (Void* KernelInterface)

Word KernelSupplier (Void* KernelInterface)

Delivers the API Version/API Flags/Kernel Id/kernel generation date/kernel version/kernel supplier.

Word NumProcessors (Void* KernelInterface)

Word NumMemoryDescriptors (Void* KernelInterface)

Delivers number of processors in the system/number of memory descriptors in the kernel-interface page.

Word PageSizeMask (Void* KernelInterface)

Word PageRights (Void* KernelInterface)

Delivers supported page sizes/page rights for the current kernel/hardware architecture.

Word ThreadIdBits (Void* KernelInterface)

Word ThreadIdSystemBase (Void* KernelInterface)
Word **ThreadIdUserBase** (Void* KernelInterface)
Delivers number of valid bits for thread numbers/lowest thread number for system threads/lowest thread number for user threads.

Word **ReadPrecision** (Void* KernelInterface)
Word **SchedulePrecision** (Void* KernelInterface)
Delivers the SYSTEMCLOCK read precision/maximal jitter for wakeups (both in µs).

Word **UtcbAreaSizeLog2** (Void* KernelInterface)
Word **UtcbAlignmentLog2** (Void* KernelInterface)
Word **UtcbSize** (Void* KernelInterface)
Delivers required minimum size of UTCB area/alignment requirement for UTCBs/size of a single UTCB.

Word **KipAreaSizeLog2** (Void* KernelInterface)
Delivers size of kernel interface page area.

Word **BootInfo** (Void* KernelInterface)
Delivers the contents of the boot info field.

Char* **KernelVersionString** (Void* KernelInterface)
Delivers the kernel version string.

Char* **Feature** (Void* KernelInterface, Word num)
Delivers the numth kernel feature string, or a null pointer if num exceeds the number of available feature strings.

MemoryDesc* **MemoryDesc** (Void* KernelInterface, Word num)
Delivers the numth memory descriptor, or a null pointer if num exceeds the number of available descriptors.

ProcDesc* **ProcDesc** (Void* KernelInterface, Word num)
Delivers the numth processor descriptor, or a null pointer if num exceeds the number of processors of the system (see ProcessorInfo).

---

**Support Functions:**

#include <l4/kip.h>

Word **UndefinedMemoryType**
Word **ConventionalMemoryType**
Word **ReservedMemoryType**
Word **DedicatedMemoryType**
Word **SharedMemoryType**
Word **BootLoaderSpecificMemoryType**
Word **ArchitectureSpecificMemoryType**

bool **IsVirtual** (MemoryDesc& m) [IsMemoryDescVirtual]
Delivers true if memory descriptor specifies a virtual memory region.

Word **Type** (MemoryDesc& m) [MemoryDescType]
Word **Low** (MemoryDesc& m) [MemoryDescLow]
Word **High** (MemoryDesc& m) [MemoryDescHigh]
Delivers type ($t\times16 + type$), low limit, and high limit of memory region.
Word \texttt{ExternalFreq} \ (\texttt{ProcDesc} \& p) \quad \text{[ProcDescExternalFreq]}

Word \texttt{InternalFreq} \ (\texttt{ProcDesc} \& p) \quad \text{[ProcDescInternalFreq]}

Delivers external frequency/internal frequency of processor.
1.3 Virtual Registers

Virtual registers are implemented by the microkernel. They offer a fast interface to exchange data between the microkernel and user threads. Virtual registers are registers in the sense that they are static per-thread objects. Dependent on the specific processor type, they can be mapped to hardware registers or to memory locations. Mixtures, some virtual registers to hardware registers, some to memory are also possible. The ABI for virtual-register access depends on the specific processor type and on the virtual-register type, see Appendices A.1, B.1 and C.1 for specific hardware details.

There are three classes of virtual registers:

- **Thread Control Registers (TCRs)**, see page 16
- **Message Registers (MRs)**, see page 44
- **Buffer Registers (BRs)**, see page 55

Loading illegal values into virtual registers, overwriting read-only virtual registers, or accessing virtual registers of other threads in the same address space (which may be physically possible if some are mapped to memory locations) is illegal and can have undefined effects on all threads of the current address space. However, since virtual registers can not be accessed across address spaces, they are safe from the kernel’s point of view: Illegal accesses can like any other programming bug only compromise the originator’s address space.

**Remark:**

In general, virtual registers can only be addressed directly, not indirectly through pointers. The generic API therefore offers no operations for indirect virtual-register access. However, processor-specific code generators might use indirect access techniques if the ABI permits it.

---

**Generic Programming Interface**

```c
#include <l4/message.h>

Void StoreMR (int i, Word& w)
Void LoadMR (int i, Word w)
  Delivers/sets MR i.

Void StoreMRs (int i, k, Word& [k] w)
Void LoadMRs (int i, k, Word& [k] w)
  Stores/loads MR i...i+k-1 to/from memory.

Void StoreBR (int i, Word& w)
Void LoadBR (int i, Word w)
  Delivers/sets the value of BR i.

Void StoreBRs (int i, k, Word& [k])
Void LoadBRs (int i, k, Word& [k])
  Stores/loads BR i...i+k-1 to/from memory.
```
Chapter 2

Threads
2.1 Thread ID [Data Type]

Thread IDs identify threads and hardware interrupts. A thread ID can be global or local. Global thread IDs are unique through the entire system. They identify threads independently of the address space in which they are used. Local thread IDs exist per address space; the scope of a thread’s local ID is only the thread’s own address space. In different address spaces, the same local thread ID may identify different and unrelated threads.

Note that any thread has a global and a local thread ID. Both global and local thread IDs are encoded in a single word.

Global Thread ID

A global thread ID consists of a word, where 18 bits (32-bit processor) or 32 bits (64-bit processor) determine the thread number and 14 bits (32-bit processor) or 32 bits (64-bit processor) are available for a version number. At least one of the lowermost 6 version bits must be 1 to differentiate a global from a local thread ID.

User-thread numbers can be freely allocated within the interval \[UserBase, 2^t\], where \(t\) denotes the upper limit of thread IDs. The thread-number interval \([SystemBase, UserBase)\) is reserved for L4-internal threads. Hardware interrupts are regarded as hardware-implemented threads. Consequently, they are identified by thread IDs. Their corresponding thread numbers are within the interval \([0, SystemBase)\). The values \(SystemBase\), \(UserBase\), and \(t\) are published in the kernel interface page (see page 4).

Global thread ID

<table>
<thead>
<tr>
<th>global thread ID</th>
<th>thread no (18/32)</th>
<th>version(14/32) ≠ 0 (mod 64)</th>
</tr>
</thead>
</table>

Global interrupt ID

<table>
<thead>
<tr>
<th>global interrupt ID</th>
<th>intr no (18/32)</th>
<th>1 (14/32)</th>
</tr>
</thead>
</table>

Global thread IDs have a version field whose content can be freely set by those threads that can create and delete threads. However, the lowermost 6 bits of the version must not all be 0, i.e. \(v \mod 64 \neq 0\) must hold for every version \(v\). For hardware interrupts, the version field is always 1.

The microkernel checks version fields whenever a thread is accessed through its global thread ID. However, the semantics of the version field are not defined by the microkernel. OS personalities are free to use this field for any purpose. For example, they may use it to make thread IDs unique in time.

Local Thread ID

Local thread IDs identify threads within the same address space. They are identified by the 6 lowermost bits being 0.

Local thread ID

<table>
<thead>
<tr>
<th>local thread ID</th>
<th>local id/64 (26/58)</th>
<th>000000</th>
</tr>
</thead>
</table>

Special Thread IDs

Special IDs exist for nilthread and two wild cards. The thread ID anythread matches with any given thread ID, including all interrupt IDs. The ID anylocalthread matches all threads that reside in the same address space.

nilthread

<table>
<thead>
<tr>
<th>nilthread</th>
<th>0 (32/64)</th>
</tr>
</thead>
</table>

anythread

<table>
<thead>
<tr>
<th>anythread</th>
<th>−1 (32/64)</th>
</tr>
</thead>
</table>

anylocalthread

<table>
<thead>
<tr>
<th>anylocalthread</th>
<th>−1 (26/58)</th>
<th>000000</th>
</tr>
</thead>
</table>
Generic Programming Interface

```c
#include <l4/thread.h>

struct THREADID { Word raw };

ThreadId nilthread
ThreadId anythread
ThreadId anylocalthread

ThreadId GlobalId (Word threadno, version) 
    Delivers a thread ID with indicated thread and version number.

Word Version (ThreadId t) 
Word ThreadNo (ThreadId t) 
    Delivers version/thread number of indicated global thread ID.
```

Convenience Programming Interface

```c
#include <l4/thread.h>

bool == (ThreadId l, r) [IsThreadEqual] 
bool != (ThreadId l, r) [IsThreadNotEqual] 
    Check if thread IDs match or differ. The result of comparing a local ID with a global ID will always indicate a mismatch, even if the IDs refer to the same thread.

bool SameThreads (ThreadId l, r) 
    { GlobalId (l) == GlobalId (r) } 
    Check if thread IDs refer to the same thread. Also works if one ID is local and the other is global.

bool IsNilThread (ThreadId t) 
    { t == nilthread } 

bool IsLocalId (ThreadId t) 
bool IsGlobalId (ThreadId t) 
    Check if thread ID is a local/global one.

ThreadId LocalId (ThreadId t) [LocalIdOf] 
ThreadId GlobalId (ThreadId t) [GlobalIdOf] 
    Delivers the local/global ID of the specified local thread. Specifying a non-local thread delivers nilthread (see EXCHANGEREGISTERS, page 18).

ThreadId MyLocalId () 
ThreadId MyGlobalId () 
    Delivers the local/global ID of the currently running thread (see TCRs, page 16).

ThreadId Myself () 
    { MyGlobalId () }
## 2.2 Thread Control Registers (TCRs)

TCRs are a fast mechanism to exchange relatively static control information between user thread and microkernel. TCRs are static non-transient per-thread registers.

<table>
<thead>
<tr>
<th>Field</th>
<th>Type</th>
<th>Access</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>VirtualSender/ActualSender</td>
<td>(32/64)</td>
<td>R/W</td>
<td>see IPC</td>
</tr>
<tr>
<td>IntendedReceiver</td>
<td>(32/64)</td>
<td>R-only</td>
<td>see IPC</td>
</tr>
<tr>
<td>XferTimeouts</td>
<td>(32/64)</td>
<td>R/W</td>
<td>see IPC</td>
</tr>
<tr>
<td>ErrorCode</td>
<td>(32/64)</td>
<td>R-only</td>
<td>see IPC</td>
</tr>
<tr>
<td>Preempt Flags</td>
<td>(8)</td>
<td>R/W</td>
<td>see Scheduling</td>
</tr>
<tr>
<td>Cop Flags</td>
<td>(8)</td>
<td>W-only</td>
<td>see Miscellaneous</td>
</tr>
<tr>
<td>ExceptionHandler</td>
<td>(32/64)</td>
<td>R/W</td>
<td>see Miscellaneous</td>
</tr>
<tr>
<td>Pager</td>
<td>(32/64)</td>
<td>R/W</td>
<td>see Protocols</td>
</tr>
<tr>
<td>UserDefinedHandle</td>
<td>(32/64)</td>
<td>R/W</td>
<td>see Threads</td>
</tr>
<tr>
<td>ProcessorNo</td>
<td>(32/64)</td>
<td>R-only</td>
<td>see Miscellaneous</td>
</tr>
<tr>
<td>MyLocalId</td>
<td>(32/64)</td>
<td>R-only</td>
<td>see Threads, IPC</td>
</tr>
<tr>
<td>MyGlobalId</td>
<td>(32/64)</td>
<td>R-only</td>
<td>see Threads, IPC</td>
</tr>
</tbody>
</table>

### MyGlobalId
Global ID of the thread.

### MyLocalId
Local ID of the thread.

### ProcessorNo
The processor number on which the thread currently executes.

### UserDefinedHandle
This field can be freely set and read by user threads. It can, e.g., be used for storing a thread number, a pointer to an additional user thread control block, etc.
Generic Programming Interface

The listed generic functions permit user code to access TCRs independently of the processor-specific TCR model. All functions are user-level functions; the microkernel is not involved.

```c
#include <l4/thread.h>

ThreadId MyLocalId ()
ThreadId MyGlobalId ()
    Delivers the local/global ID of the currently running thread (see TCRs, page 16).

ThreadId Myself ()
    { MyGlobalId () }

int ProcessorNo ()
    Delivers the processor number the current thread is running on. Delivered value is a valid index into the processor description array (see Kernel Interface Page, page 4).

Word UserDefinedHandle ()
Void Set_UserDefinedHandle (Word NewValue)
    Delivers/sets the user defined handle of the currently running thread.

ThreadId Pager ()
Void Set_Pager (ThreadId NewPager)
    Delivers/sets the pager for the currently running thread.

ThreadId ExceptionHandler ()
Void Set_ExceptionHandler (ThreadId NewHandler)
    Delivers/sets the exception handler for the currently running thread.

Void Set_CopFlag (Word n)
Void Clr_CopFlag (Word n)
    Sets/clears coprocessor flag c_n.

Word ErrorCode ()
    Delivers the error code of the last IPC (see IPC, page 60).

Word XferTimeouts ()
Void Set_XferTimeouts (Word NewValue)
    Delivers/sets the transfer timeouts for the currently running thread (see IPC, page 59).

ThreadId IntendedReceiver ()
    Delivers the intended receiver of last received IPC (see IPC, page 60).

ThreadId ActualSender ()
    Delivers the actual sender of the last propagated IPC (see IPC, page 59).

Void Set_VirtualSender (ThreadId t)
    Sets the virtual sender for the next deceiving IPC (see IPC, page 59).
```

Code generators of IDL and other compilers are not restricted to the generic interface. They can use any processor-specific methods and optimizations to access TCRs.
2.3 **ExchangeRegisters** [Systemcall]

<table>
<thead>
<tr>
<th>Input Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>dest</strong></td>
</tr>
<tr>
<td><strong>control</strong></td>
</tr>
<tr>
<td><strong>h p u f i s</strong></td>
</tr>
<tr>
<td><strong>S R</strong></td>
</tr>
</tbody>
</table>

Exchanges or reads a thread’s *FLAGS*, *SP*, and *IP* hardware registers as well as *pager* and UserDefinedHandle TCRs. Furthermore, thread execution can be suspended or resumed. The destination thread must exist and must reside in the invoker’s address space.

Any *IP*, *SP*, or *FLAGS* modification changes the corresponding *user-level* registers of the addressed thread. In general, ongoing kernel activities are not influenced. However, a currently active IPC operation can be canceled or aborted. For details see the *SR*-bit specification below.

Modifications of the *pager* TCR and the *UserDefinedHandle* TCR become immediately effective, whether the destination thread executes in user mode or in kernel mode.
EXCHANGEREGISTERS

$H = 1$ User-level thread execution is halted. Note that ongoing IPCs and other kernel operations are not affected by $H$. (See $SR$ for also aborting active IPC.)

$SP$ The current user-level stack pointer is set to $SP$ if $s = 1$. Ignored for $s = 0$.

$IP$ The current user-level instruction pointer is set to $IP$ if $i = 1$. If the thread was stopped/inactive before and resumed by $h = 1 \land H = 0$, it is implicitly started. Ignored for $i = 0$.

$FLAGS$ Sets the user-level processor flags of the thread if $f = 1$. Ignored for $f = 0$. The semantics of the $FLAGS$ word depend on the processor type.

$UserDefinedHandle$ Sets the thread’s $UserDefinedHandle$ TCR if $u = 1$. Ignored for $u = 0$.

$pager$ Sets the thread’s $pager$ TCR if $p = 1$. Ignored for $p = 0$.

Output Parameters

$\text{result} \neq \text{nilthread}$, input parameter dest was a local thread ID
global thread ID of the addressed thread. EXCHANGEREGISTERS succeeded.

$\text{result} \neq \text{nilthread}$, input parameter dest was a global thread ID
local thread ID of the addressed thread. EXCHANGEREGISTERS succeeded.

$\text{result} = \text{nilthread}$ Operation failed. dest might denote a thread that resides in a different address space or might denote no existing thread.

$control$

\begin{tabular}{|c|c|}
\hline
0 (29/61) & $S RH$ \\
\hline
\end{tabular}

$H$ Reports whether the addressed thread was halted ($H = 1$) or not ($H = 0$) when EXCHANGEREGISTERS was invoked. Note that this output $control$ bit is independent of the input parameter $control$.

$SR$ Reports whether the addressed thread was within an IPC operation when EXCHANGEREGISTERS was invoked. A value of 0 reports that the addressed thread was not within a send phase ($S = 0$) or not within a receive phase ($R = 0$), respectively. Note that these output $control$ bits are independent of the input parameter $control$.

$R = 1$ Operation was executed while the addressed thread was within the receive phase of an IPC operation. If the input control word had $R = 1$ the IPC operation was canceled or aborted.

$S = 1$ Operation was executed while the addressed thread was within the send phase of an IPC operation. If the input control word had $S = 1$ the IPC operation was canceled or aborted.

$SP$ Old user-level stack pointer of the thread.

$IP$ Old user-level instruction pointer of the thread.
**FLAGS**
Old user-level flags of the thread. The semantics of this word is processor specific.

---

**UserDefinedHandle**
Old content of thread’s UserDefinedHandle TCR.

---

**pager**
Old content of thread’s pager TCR.

---

**Pagefaults**
No pagefaults will happen.

---

**Generic Programming Interface**

**System-Call Function:**

```c
#include <l4/thread.h>

ThreadId ExchangeRegisters (ThreadId dest, Word control, sp, ip, flags, UserDefinedHandle, ThreadId pager, Word& old_control, old_sp, old_ip, old_flags, old_UserDefinedHandle, ThreadId& old_pager)
```

**Convenience Programming Interface**

**Derived Functions:**

```c
#include <l4/thread.h>

ThreadId GlobalId (ThreadId t) [GlobalIdOf]
    { if (IsLocalId (t)) ExchangeRegisters (t,0,−…−) else t }

    Delivers global ID of specified local thread. Specifying a non-local thread delivers nilthread.

ThreadId LocalId (ThreadId t) [LocalIdOf]
    { if (IsGlobalId (t)) ExchangeRegisters (t,0,−…−) else t }

    Delivers local ID of specified local thread. Specifying a non-local thread delivers nilthread.

Word UserDefinedHandle (ThreadId t) [UserDefinedHandleOf]

Void Set_UserDefinedHandle (ThreadId t, Word handle) [Set_UserDefinedHandleOf]
    Delivers/sets the user defined handle of specified local thread. Result of specifying a non-local thread is undefined.

ThreadId Pager (ThreadId t) [PagerOf]

Void Set_Pager (ThreadId t, p) [Set_PagerOf]
    Delivers/sets the pager for specified local thread. Result of specifying a non-local thread is undefined.

Void Start (ThreadId t) [Start]

Void Start (ThreadId t, Word sp, ip) [Start_SpIp]

Void Start (ThreadId t, Word sp, ip, flags) [Start_SpIpFlags]
    Resume execution of specified local thread (if halted). Optionally modify stack pointer, instruction pointer, and processor flags according to function parameters. Result of specifying a non-local thread is undefined.
ThreadState Stop (ThreadId t)
ThreadState Stop (ThreadId t, Word& sp, ip, flags)  [Stop_SpIpFlags]
Halt execution of specified local thread and return its current thread state. Do not abort any on-
going IPC operation. Optionally return thread’s stack pointer, instruction pointer, and processor
flags in output parameters. Result of specifying a non-local thread is undefined.

ThreadState AbortReceive_and_stop (ThreadId t)
ThreadState AbortReceive_and_stop (ThreadId t, Word& sp, ip, flags)  [AbortReceive_and_stop_SpIpFlags]
As stop (), except any ongoing IPC receive operation is immediately aborted.

ThreadState AbortSend_and_stop (ThreadId t)
ThreadState AbortSend_and_stop (ThreadId t, Word& sp, ip, flags)  [AbortSend_and_stop_SpIpFlags]
As stop (), except any ongoing IPC send operation is immediately aborted.

ThreadState AbortIpc_and_stop (ThreadId t)
ThreadState AbortIpc_and_stop (ThreadId t, Word& sp, ip, flags)  [AbortIpc_and_stop_SpIpFlags]
As stop (), except any ongoing IPC send or receive operations are immediately aborted.

Support Functions:

#include <l4/thread.h>

struct THREADSTATE { Word raw }

bool ThreadWasHalted (ThreadState s)
bool ThreadWasSending (ThreadState s)
bool ThreadWasReceiving (ThreadState s)
bool ThreadWasIpcing (ThreadState s)

Query the thread state returned from one of the stop () functions.
2.4 THREADCONTROL  [Privileged Systemcall]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>dest</td>
<td>Addressed thread. Must be a global thread ID. Only the thread number is effectively used to address the thread. If a thread with the specified thread number exists, its version bits are overwritten by the version bits of dest id and any ongoing IPC operations are aborted. Otherwise, the specified version bits are used for thread creations, i.e., a thread creation generates a thread with ID dest.</td>
</tr>
<tr>
<td>SpaceSpecifier</td>
<td>Creation. The space specifier specifies in which address space the thread will reside. Since address space do not have own IDs, a thread ID is used as SpaceSpecifier. Its meaning is: the new thread should execute in the same address space as the thread SpaceSpecifier. The first thread in a new address space is created with SpaceSpecifier = dest. This operation implicitly creates a new empty address space. Note that the space creation must be completed by a SPACECONTROL operation before the thread(s) can execute.</td>
</tr>
<tr>
<td>scheduler</td>
<td>Modification Only. The addressed thread dest is neither deleted nor created. Modifications can change the version bits of the thread ID, the associated scheduler, the pager, or the associated address space, i.e., migrate the thread to a new address space.</td>
</tr>
<tr>
<td>pager</td>
<td>Deletion. The addressed thread dest is deleted. Deleting the last thread of an address space implicitly also deletes the address space.</td>
</tr>
<tr>
<td>Void*</td>
<td>Defines the scheduler thread that is permitted to schedule the addressed thread. Note that the scheduler thread must exist when the addressed thread starts executing.</td>
</tr>
</tbody>
</table>

A privileged thread, e.g., the root server, can delete and create threads through this function. It can also modify the global thread ID (version field only) of an existing thread.

Threads can be created as active or inactive threads. Inactive threads do not execute but can be activated by active threads that execute in the same address space.

An actively created thread starts immediately by executing a short receive operation from its pager. (An active thread must have a pager.) The actively started thread expects a start message (MsgTag and two untyped words) from its pager. Once it receives the start message, it takes the value of MR₁ as its new IP, the value of MR₂ as its new SP, and then starts execution at user level with the received IP and SP.

Interrupt threads are treated as normal threads. They are active at system startup and can not be deleted or migrated into a different address space (i.e., SpaceSpecifier must be equal to the interrupt thread ID). When an interrupt occurs the interrupt thread sends an IPC to its pager and waits for an empty end-of-interrupt acknowledgment message (MR₀=0). Interrupt threads never raise pagefaults. To deactivate interrupt message delivery the pager is set to the interrupt thread’s own ID.
**scheduler = nilthread**
The current scheduler association is not modified. This variant is illegal for a creating THREADCONTROL operation.

**pager ≠ nilthread**
The pager of dest is set to the specified thread. If dest was inactive before, it is activated.

**pager = nilthread**
The current pager association is not modified. If used with a creating THREADCONTROL operation, dest is created as an inactive thread.

**UtcbLocation ≠ -1**
The start address of the UTCB of the thread is set to UtcbLocation. The UTCB must fit entirely into the UTCB area of the configured address space, and must be properly aligned according to the UtcbInfo field of the kernel interface page. It is the application’s responsibility to ensure that UTCBs of multiple threads do not overlap. Changing the UtcbLocation of an already active thread is an illegal operation.

**UtcbLocation = -1**
The UTCB location is not modified.

**UtcbInfo [KernelInterfacePage Field]**
Permits to calculate the appropriate page size of the UTCB area fpage and specifies the size and alignment of UTCBs. Note that the size restricts the total number of threads that can reside in an address space.

\[
\begin{array}{cccc}
\sim (10/42) & s (6) & a (6) & m (10) \\
\end{array}
\]

- **s** The minimal area size for an address space’s UTCB area is \(2^s\). The size of the UTCB area limits the total number of threads \(k\) to \(2^s mk \leq 2^s\).
- **m** UTCB size multiplier.
- **a** The UTCB location must be aligned to \(2^a\). The total size required for one UTCB is \(2^a m\).

**Output Parameters**

**result**
The result is 1 if the operation succeeded completely, 0 otherwise. (The operation may fail because the addressed thread does not exist, UtcbLocation is not valid, and/or the invoker is not sufficiently privileged for the requested operation.)

**Pagefaults**
No pagefaults will happen.

**Generic Programming Interface**

**System-Call Function:**

```c
#include <l4/thread.h>

Word ThreadControl (ThreadId dest, SpaceSpecifier, Scheduler, Pager, Void* UtcbLocation)
```
Convenience Programming Interface

Derived Functions:

```
#include <l4/thread.h>

Word AssociateInterrupt (ThreadId InterruptThread, InterruptHandler)
    { ThreadControl (InterruptThread, InterruptThread, nilthread, InterruptHandler, -1) }

    Associate a handler thread with the specified interrupt source.

Word DeassociateInterrupt (ThreadId InterruptThread)
    { ThreadControl (InterruptThread, InterruptThread, nilthread, InterruptThread, -1) }

    Remove association between the specified interrupt source and any potential handler thread.
```
Chapter 3

Scheduling
3.1 Clock [Data Type]

On both 32-bit and 64-bit processors, the system clock is represented as a 64-bit unsigned counter. The clock measures time in 1 µs units, independent of the processor frequency. Although the clock base is undefined, it is guaranteed that the counter will not overflow for at least 1,000 years.

---

**Generic Programming Interface**

```c
#include <l4/schedule.h>

struct Clock {
    Word64 raw
};
```

---

**Convenience Programming Interface**

```c
#include <l4/schedule.h>

Clock + (Clock l, int r)  \[ClockAddUsec\]
Clock + (Clock l, Word64 r)  \[ClockAddUsec\]
Clock − (Clock l, int r)  \[ClockSubUsec\]
Clock − (Clock l, Word64 r)  \[ClockSubUsec\]
```

Adds/subtracts a number of µs to/from a clock value. Delivers new clock value. Does not modify the old clock value.

```c
bool < (Clock l, r)  \[IsClockEarlier\]
bool > (Clock l, r)  \[IsClockLater\]
bool <= (Clock l, r)  \[IsClockEqual\]
bool >= (Clock l, r)  \[IsClockNotEqual\]
bool != (Clock l, r)  \[IsClockNotEqual\]
```

Compares two clock values.
3.2 **SYSTEMCLOCK**  [Systemcall]

\[ \rightarrow \quad \text{Clock} \quad \text{clock} \]

Delivers the current system clock. Typically, the operation does not enter kernel mode.

---

**Pagefaults**

No pagefaults will happen.

---

**Generic Programming Interface**

**System-Call Function:**

```c
#include <l4/schedule.h>

Clock SystemClock ()
```

---
3.3 Time [Data Type]

Time values are used to specify send/receive timeouts for IPC operations (see page 58) and time quanta for scheduling (see page 31). The unit for time periods as well as for time points is 1 µs. Clock ticks thus happen every µs.

Relative time values specify a time period. Time periods are encoded as un-normalized 16-bit floating-point numbers. (Note that for easier handling the mantissa can have leading 0-bits.) The shortest non-zero time period that can be specified is 1 µs, the longest finite period slightly exceeds 610 hours. Two special periods frequently used for timeouts are 0 and ∞, a never ending period. The values 0 and ∞ have special encodings.

\[
\begin{align*}
\text{time period:} & \quad 0 \begin{pmatrix} e \ (5) \ m \ (10) \end{pmatrix} = 2^e m \ \mu s \\
& \quad 0 \begin{pmatrix} 0 \ (16) \end{pmatrix} = \infty \\
& \quad 0 \begin{pmatrix} 1 \ (5) \ 0 \ (10) \end{pmatrix} = 0
\end{align*}
\]

Absolute time values specify a point in time. They are only valid for a limited period, at maximum 67 seconds.

\[
\begin{pmatrix} 1 \ e \ (4) \ c \ m \ (10) \end{pmatrix}
\]

For a semantical description of time-point values, we use \textit{Clock} to denote the current clock value in µs, \(x_{[i]}\) to denote bit \(i\) of \(x\), and \(x_{[i,j]}\) to denote the number consisting of bits \(i\) to \(j\) of \(x\). Then, the time-point value \((c, m, e)\) specifies the point:

\[
t = \begin{cases} 
2^e \cdot (m + \text{Clock}_{[63,e+9]} \cdot 2^{10}) & \text{if } \text{Clock}_{[e+10]} = c \\
2^e \cdot (m + \text{Clock}_{[63,e+9]} \cdot 2^{10} + 2^{10}) & \text{if } \text{Clock}_{[e+10]} \neq c
\end{cases}
\]

Absolute time values are thus the more precise the nearer in the future they are.

Absolute time values with maximal precision become invalid just after the clock has reached the specified point in time. The validity interval can be expanded, but only by reducing the precision. In general, a time-point value \((c, m, e)\) that is constructed when the current clock value is \(C_0\) is valid from \(C_0\) up to

\[
C_0 + (2^{10} - 1) \cdot 2^e
\]

Therefore, a time-point value that should remain valid for 10 ms can have a precision of 10 µs whereas a value that should remain valid for an entire second can only have a precision of 1 ms. In general, a precision of 0.1% of the required validity interval can be achieved.

---

**Generic Programming Interface**

```c
#include <l4/schedule.h>

struct TIME { Word16 raw }

Time Never

Time ZeroTime

Time TimePeriod (Word64 microseconds)
```
**Convenience Programming Interface**

```c
#include <l4/schedule.h>

Time + (Time l, Word r) \[ TimeAddUsec \]
Time += (Time l, Word r) \[ TimeAddUsecTo \]
Time − (Time l, Word r) \[ TimeSubUsec \]
Time −= (Time l, Word r) \[ TimeSubUsecFrom \]

Time + (Time l, r) \[ TimeAdd \]
Time += (Time l, r) \[ TimeAddTo \]
Time − (Time l, r) \[ TimeSub \]
Time −= (Time l, r) \[ TimeSubFrom \]

bool > (Time l, r) \[ IsTimeLonger \]
bool >= (Time l, r) \[ IsTimeLongerOrEqual \]
bool < (Time l, r) \[ IsTimeShorter \]
bool <= (Time l, r) \[ IsTimeShorterOrEqual \]
bool == (Time l, r) \[ IsTimeEqual \]
bool != (Time l, r) \[ IsTimeNotEqual \]
```

Adds/subtracts a number of microseconds to/from a time value.

Adds/subtracts a time period to/from a time value. The result of adding/subtracting a time point is undefined.

Compares two time values. The result of comparing a time period with a time point, or vice versa, is undefined.
3.4 THREADSWITCH [Systemcall]

ThreadId dest → Void

The invoking thread releases the processor (non-preemptively) so that another ready thread can be processed.

Input Parameter

dest = nilthread

Processing switches to an undefined ready thread which is selected by the scheduler. (It might be the invoking thread.) Since this is “ordinary” scheduling, the thread gets a new timeslice.

dest ≠ nilthread

If dest is ready, processing switches to this thread. In this “extraordinary” scheduling, the invoking thread donates its remaining timeslice to the destination thread. (This one gets the donation in addition to its ordinarily scheduled timeslices, if any.)

If the destination thread is not ready or resides on a different processor, the system call operates as described for dest = nilthread.

Pagefaults

No pagefaults will happen.

Generic Programming Interface

System-Call Function:

```c
#include <l4/schedule.h>

Void ThreadSwitch (ThreadId dest)
```

Convenience Programming Interface

Derived Functions:

```c
#include <l4/schedule.h>

Void Yield ()

{ ThreadSwitch (nilthread) }

Switch processing to a thread selected by the scheduler.
3.5 **SCHEDULE**  [Systemcall]

<table>
<thead>
<tr>
<th>ThreadId</th>
<th>dest</th>
<th>→</th>
<th>Word</th>
<th>result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Word</td>
<td>time control</td>
<td>Word</td>
<td>time control</td>
<td></td>
</tr>
<tr>
<td>Word</td>
<td>processor control</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Word</td>
<td>prio</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Word</td>
<td>preemption control</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The system call can be used by schedulers to define the **priority**, **timeslice length**, and other scheduling parameters of threads. Furthermore, it delivers thread states.

The system call is only effective if the calling thread is defined as the destination thread’s scheduler (see thread control, page 22).

---

**Input Parameters**

**dest**

Destination thread ID. The destination thread must be existent (but can be inactive) and the current thread must be defined as the destination thread’s scheduler (see thread control). Otherwise, the destination thread is not affected.

All further input parameters have no effect if the supplied value is $-1$, ensuring that the corresponding internal thread variable is *not* modified. The following description always refers to values $\neq -1$.

---

**time control**

| ts len (16) | total quantum (16) |

New timeslice length for the destination thread. The timeslice length is specified as a time period (see page 28). Absolute time values and the value 0 are illegal. A timeslice length of $\infty$, however, can be specified. In that case, the thread never experiences a preemption due to exhausted time slice. The specified value is always rounded up to the nearest possible timeslice length. In particular, a time period of $1\,\mu s$ results in the shortest possible timeslice.

Writing the timeslice length initializes the current quantum with the new length. After the quantum is exhausted, the thread is preempted while the quantum is reloaded with $ts\, len$ for the next timeslice.

**total quantum**

Defines the total quantum for the thread. Exhaustion of the total quantum results in an RPC to the thread’s scheduler (i.e., the current thread). (Re)writing the total quantum re-initializes the quantum, independent of the already consumed total quantum. The total quantum is specified as a time period (see page 28). Absolute time values are illegal. A total quantum of $\infty$ can be specified.

---

**prio**

| 0 (24/56) | prio (8) |

New priority for destination thread. Must be less than or equal to current thread’s priority.

---

**preemption control**

| 0 (8/40) | sensitive prio (8) | maximum delay (16) |

**sensitive prio**

Preemptions by threads that run on a priority lower or equal to this sensitive prio will, (a) if the delay-preemption flag is set, be delayed until the thread executes a thread switch (nilthread) system call; and (b) if the signal-preemption flag is set, raise a preemption fault to the exception handler.

No preemption delays or signaling will occur if preempted by a thread having a higher priority than sensitive prio, regardless of the state of the delay-preemption and signal-preemption flags.
**maximum delay**

The maximum time in µs a pending preemption can be delayed in the destination thread. The value 0 effectively disables preemption delay.

**processor control**

| 0 (16/48) | processor number (16) |

**processor number**

Specifies the processor number to which the thread should be migrated. The processor number must be valid, i.e., smaller than the total number of processors (see kernel interface page at page 3). Otherwise, the parameter is ignored. The first processor number is denoted as 0.

---

**Output Parameters**

| result | ~ (24/56) | tstate (8) |

**tstate**

- **0**  
  *Error*. The operation failed completely. The invoker has specified invalid parameters or is not sufficiently privileged for the requested operation.

- **1**  
  *Dead*. The thread is unable to execute or does not exist.

- **2**  
  *Inactive*. The thread is inactive/stopped.

- **3**  
  *Running*. The thread is ready to execute at user-level.

- **4**  
  *Pending send*. A user-invoked IPC send operation currently waits for the destination (recipient) to become ready to receive.

- **5**  
  *Sending*. A user-invoked IPC send operation currently transfers an outgoing message.

- **6**  
  *Waiting to receive*. A user-invoked IPC receive operation currently waits for an incoming message.

- **7**  
  *Receiving*. A user-invoked IPC receive operation currently receives an incoming message.

**time control**

| rem ts (16) | rem total (16) |

**rem ts**

Remainder of the current timeslice.

**rem total**

Remaining total quantum of the thread.

---

**Pagefaults**

No pagefaults will happen.
Generic Programming Interface

System-Call Function:

```c
#include <l4/schedule.h>

Word Schedule (ThreadId dest, Word TimeControl, ProcessorControl, prio, PreemptionControl, Word& old_TimeControl)
```

Convenience Programming Interface

Derived Functions:

```c
#include <l4/schedule.h>

Word Set_Priority (ThreadId dest, Word prio)
{ Schedule (dest, -1, -1, prio, -1) }

Word Set_ProcessorNo (ThreadId dest, Word ProcessorNo)
{ Schedule (dest, -1, ProcessorNo, -1, -1) }

Word Timeslice (ThreadId dest, Time & ts, Time & tq)
Delivers the remaining timeslice and total quantum of the given thread.

Word Set_Timeslice (ThreadId dest, Time ts, Time tq)
{ Schedule (dest, ts * 2^16 + tq, -1, -1, -1) }

Word Set_PreemptionDelay (ThreadId dest, Word sensitivePrio, Word maxDelay)
{ Schedule (dest, -1, -1, -1, SensitivePrio * 2^16 + MaxDelay) }
```
3.6 Preempt Flags [TCR]

The *preemption flags* TCR controls asynchronous preemptions (timeslice exhausted or activation of a higher-priority thread including device interrupts).

**Preempt Flags**

<table>
<thead>
<tr>
<th>I</th>
<th>d</th>
<th>s</th>
</tr>
</thead>
</table>

The *ds*-flags are used to control the microkernel. User threads can set/reset them. The *I*-flag signals an event to the user. It is set by the microkernel and typically read/reset by the user.

- **s = 0**
  Asynchronous preemptions are not signaled to the exception handler.

- **s = 1**
  Asynchronous preemptions are signaled as preemption faults to the exception handler. If *d = 0* this happens immediately. Otherwise, it is delayed until the thread continues execution after the preemption.

- **d = 0**
  All asynchronous preemptions happen immediately. If they are signaled as preemption faults (*s = 1*), this happens after the preemption took place, i.e., when the thread gets reactivated.

- **d = 1**
  Asynchronous preemptions are delayed if the priority of the preemptor is lower or equal than the *sensitive priority* for the current thread. (The sensitive priority is set by the scheduler, see page 31.) A delayed preemption does not interrupt the current thread immediately but is postponed until the current thread invokes a systemcall *thread switch* (*nilthread*). However, a pending preemption must not be delayed for longer than the *maximum delay* that was set by the thread’s scheduler. Such a preemption-delay overflow resets the *d*-bit and is signaled to the exception handler.

- **I = 0**
  No asynchronous preemption is pending.

- **I = 1**
  An asynchronous preemption is currently pending, i.e., the thread should as soon as possible reset the *d*-flag and invoke *thread switch*. Invoking *thread switch* re-enables the *maximum delay* for the next delayed asynchronous preemption. Invoking *thread switch* is not required if no asynchronous preemption is pending (*I = 0*) after the user thread has reset the *d*-flag.

---

**Generic Programming Interface**

```c
#include <l4/schedule.h>

bool EnablePreemptionFaultException ()

bool DisablePreemptionFaultException ()
    Sets/resets the *s*-flag and delivers the old *s*-flag value (true = set).

bool DisablePreemption ()

bool EnablePreemption ()
    Sets/resets the *d*-flag and delivers the old *d*-flag value (true = set).

bool PreemptionPending ()
    Resets the *I*-flag and delivers the old *I*-flag value (true = set).
```
Chapter 4

Address Spaces and Mapping
4.1 Fpage [Data Type]

Fpages (Flexpages) are regions of the virtual address space. An fpage consists of all pages mapped actually in this region sans kernel mapped objects, i.e., kernel interface page and UTCBs. Fpages have a size of at least 1 K. For specific processors, the minimal fpage size may be larger; e.g., a Pentium processor offers a minimal page size of 4 K while the Alpha processor offers smallest pages of 8 K. Fpages smaller than the minimal page size are treated as nilpages. The kernel interface page (see page 3) specifies which page sizes are supported by the hardware/kernel. An fpage of size \(2^s\) has a \(2^s\)-aligned base address \(b\), i.e., \(b \equiv 0 \pmod{2^s}\), where \(s \geq 10\) for all architectures.

Mapped fpages are considered inseparable objects. That is, if an fpage is mapped, the mapper can not later partially unmap the mapped page; the whole fpage must be unmapped in a single operation. The mappee can, however, separate the fpage and map fpages (objects) of smaller size. Partially unmapping an fpage might or might not work on some systems. The kernel will give no indication as to whether such an operation succeeded or not.

\[
\text{fpage } (b, \ 2^s) = \begin{array}{c}
\begin{array}{c}
0_{(22/54)}
\end{array}
\end{array}
\begin{array}{c}
\begin{array}{c}
s = 1_{(6)}
\end{array}
\end{array}
\begin{array}{c}
0_{rwx}
\end{array}
\]

Special fpage denoters describe the complete user address space and the nilpage, an fpage which has no base address and a size of 0:

\[
\begin{array}{c}
\text{complete}
\end{array}
\begin{array}{c}
0_{(22/54)}
\end{array}
\begin{array}{c}
\begin{array}{c}
s = 1_{(6)}
\end{array}
\end{array}
\begin{array}{c}
0_{rwx}
\end{array}
\]

\[
\begin{array}{c}
\text{nilpage}
\end{array}
\begin{array}{c}
0_{(32/64)}
\end{array}
\]

Access Rights

The \(rwx\) bits define the accessibility of the fpage:

\[
\begin{array}{c}
r \quad \text{readable}
\end{array}
\begin{array}{c}
w \quad \text{writable}
\end{array}
\begin{array}{c}
x \quad \text{executable}
\end{array}
\]

A bit set to one permits the corresponding access to the newly-mapped/granted page provided that the mapper itself possesses that access right. If the mapper does not have the access right itself or if the bit is set to zero the mapped/granted page will not get the corresponding access right.

Note that processor architectures may impose restrictions on the access-right combinations. However, read-only (including execute), \(rwx = 101\), and read/write/execute, \(rwx = 111\), should be valid for any processor architecture. The kernel interface page (see page 3) specifies which access rights are supported in the processor architecture.

---

**Generic Programming Interface**

```c
#include <l4/space.h>

struct FPAGE { Word raw }

Word Readable
Word Writable
```
**Word** eXecutable
**Word** FullyAccessible
**Word** ReadeXecOnly
**Word** NoAccess

**Fpage** Nilpage
**Fpage** CompleteAddressSpace

```c
bool IsNilFpage (Fpage f)
{
    f == Nilpage
}
```

**Fpage** Fpage (Word BaseAddress, int FpageSize ≥ 1K)
**Fpage** FpageLog2 (Word BaseAddress, int Log2FpageSize < 64)

Delivers an fpage with the specified location and size.

**Word** Address (Fpage f)
**Word** Size (Fpage f)
**Word** SizeLog2 (Fpage f)

Delivers address/size of specified fpage.

**Word** Rights (Fpage f)

**Void** SetRights (Fpage f, Word AccessRights)

Delivers/sets the access rights for the specified fpage.

**Fpage** + (Fpage f, Word AccessRights) [FpageAddRights]
**Fpage** += (Fpage f, Word AccessRights) [FpageAddRightsTo]
**Fpage** − (Fpage f, Word AccessRights) [FpageRemoveRights]
**Fpage** -= (Fpage f, Word AccessRights) [FpageRemoveRightsFrom]

Adds/removes specified access rights from fpage. Delivers new fpage value.
4.2 **UNMAP**  

**[Systemcall]**

\[
\text{Word control} \quad \rightarrow \quad \text{Void}
\]

The specified fpages (located in MR 0...) are unmapped. Fpages are mapped as part of the IPC operation (see page 57).

---

**Input Parameters**

<table>
<thead>
<tr>
<th>control</th>
</tr>
</thead>
<tbody>
<tr>
<td>(0) (25/57) &amp; (k) (6)</td>
</tr>
</tbody>
</table>

- \(k\) specifies the highest MR \(k\) that holds an fpage to be unmapped. The number of fpages is thus \(k + 1\).
- \(f = 0\) The fpages are unmapped recursively in all address spaces in which threads of the current address space have mapped them before. However, the fpages remain unchanged in the current address space.
- \(f = 1\) The fpages are unmapped like in the \(f = 0\) case and, in addition, also in the current address space.

**FpageList MR 0...k**  Fpages to be processed.

<table>
<thead>
<tr>
<th>Fpage MR</th>
</tr>
</thead>
<tbody>
<tr>
<td>fpage (28/58) &amp; 0 r w x</td>
</tr>
</tbody>
</table>

Fpage to be unmapped. (The term *unmapped* is used even if effectively no access right is removed.) A nilpage specifies a no-op.

- \(0 r w x\) Any access bit set to 1 revokes the corresponding access right. A 0-bit specifies that the corresponding access right should not be affected. Typical examples:
  - =0111 Complete unmap of the fpage.
  - =0010 Partial unmap, revoke writability only. As a result, the fpage is set to read-only.
  - =0000 No unmap. This case is particularly useful if only *dirty* and *accessed* bits should be read and reset without changing the mapping.

---

**Output Parameters**

**FpageList MR 0...k** The accessed status bits in the fpages are updated.
The status bits Referenced, Written, and executed of all pages processed by the unmap operation are reset and the bitwise OR-ed old values of all the processed pages are delivered in MR_{0..k}. For processors that do not differentiate between read access and execute access, the R and X bits are unified: either both are set or both are reset. Resetting status bits is not a recursive operation. However, the status bit values for pages within the current space will also reflect accesses performed on recursive mappings.

\( R = 0 \)

No part of the fpage has been Referenced after the last unmap operation (or after the initial map operation). This includes all recursively mapped pages.

**Remark:** The meaning of referenced slightly differs from read. Not being referenced means that not only no read access but that also no write and execute access occurred.

\( R = 1 \)

At least one page of the specified fpage (including all recursive mappings) has been referenced after the last unmap operation (or after the initial map operation). All in-kernel R bits are reset.

**Remark:** The meaning of referenced slightly differs from read. Write accesses and execute accesses also set the R bit.

\( W = 0 \)

No part of the fpage has been written after the last unmap operation (or after the initial map operation), i.e., the fpage is clean. This includes all recursively mapped pages.

\( W = 1 \)

At least one page of the specified fpage (including all recursive mappings) has been written after the last unmap operation (or after the initial map operation), i.e., the fpage is dirty. All in-kernel dirty bits are reset.

\( X = 0 \)

No part of the fpage has been executed after the last unmap operation (or after the initial map operation). This includes all recursively mapped pages.

\( X = 1 \)

At least one page of the specified fpage (including all recursive mappings) has been executed after the last unmap operation (or after the initial map operation). All in-kernel X bits are reset.

**Remark:** For processors that do not differentiate between read and execute accesses, the X bit is set to 1 iff \( R = 1 \).

---

**Pagefaults**

No pagefaults will happen.

---

**Generic Programming Interface**

**System-Call Function:**

```
#include <l4/space.h>

Void Unmap (Word control)
```

**Convenience Programming Interface**

**Derived Functions:**

```
#include <l4/space.h>

Void Unmap (Fpage f) [UnmapFpage]
    { LoadMR (0, f); Unmap (0); StoreMR (0, f); }

Void Unmap (Word n, Fpage &[n].fpages) [UnmapFpages]
    { LoadMRs (0, n, fpages); Unmap (n – 1); StoreMRs (0, n, fpages); }
```

Recursively unmaps the specified fpage(s) from all address spaces except the current one.
Void Flush (Fpage f)
    { LoadMR (0, f); Unmap (64); StoreMR (0, f); }

Void Flush (Word n, Fpage& [n] fpages) [FlushFpages]
    { LoadMRs (0, n, fpages); Unmap (64 + n - 1); StoreMRs (0, n, fpages); }

Recursively unmaps the specified fpage(s) from all address spaces, including the current one.

Fpage GetStatus (Fpage f)
    { LoadMR (0, f - FullyAccessible); Unmap (0); StoreMR (0, f); f }

Resets and delivers the status bits of the specified fpage.

bool WasReferenced (Fpage f)
bool WasWritten (Fpage f)
bool WasExecuted (Fpage f)

Checks the status bits of specified fpage. The specified fpage must be the output of an Unmap (), Flush (), or GetStatus () function.
4.3 **SPACECONTROL** [Privileged Systemcall]

\[
\begin{array}{c|c|c}
\text{ThreadId} & \text{SpaceSpecifier} & \rightarrow \text{Word} \\
\text{control} & \text{control} & \text{result} \\
\text{Fpage} & \text{KernelInterfacePageArea} \\
\text{Fpage} & \text{UtcArea} \\
\text{ThreadId} & \text{Redirector}
\end{array}
\]

A privileged thread, e.g., the root server, can configure address spaces through this function.

---

**Input Parameters**

**SpaceSpecifier**

Since address spaces do not have ids, a thread ID is used as *SpaceSpecifier*. It specifies the address space in which the thread resides. The *SpaceSpecifier* thread must exist although it may be inactive or not yet started. In particular, the thread may reside in an empty address space that is not yet completely created.

**KernelInterfacePageArea**

Specifies the fpage where the kernel should map the kernel interface page. The supplied fpage must have a size specified in the *KipAreaInfo* field of the kernel interface page and must fit entirely into the user-accessible part of the address space. Address 0 of the kernel interface page is mapped to the fpage’s base address. The value is ignored if there is at least one active thread in the address space.

**KipAreaInfo** [KernelInterfacePage Field]

Permits calculation of the appropriate page size of the KernelInterface area fpage.

\[
\begin{array}{c|c}
\sim (25/58) & s (6) \\
\end{array}
\]

The size of the kernel interface page area is \(2^s\).

**UtcArea**

Specifies the fpage where the kernel should map the UTCBs of all threads executing in the address space. The fpage must fit entirely into the user-accessible part of an address space. The fpage size has to be at least the smallest supported hardware-page size. In fact, the size of the UTCB area restricts the maximum number of threads that can be created in the address space. See the kernel interface page for the space and alignment that is required for UTCBs. The value is ignored if there is at least one active thread in the address space.

**UtcInfo** [KernelInterfacePage Field]

Permits to calculate the appropriate page size of the UTCB area fpage and specifies the size and alignment of UTCBs. Note that the size restricts the total number of threads that can reside in an address space.

\[
\begin{array}{c|c|c|c}
\sim (10/42) & s (6) & n (6) & m (10) \\
\end{array}
\]

The minimal area size for an address space’s UTCB area is \(2^s\). The size of the UTCB area limits the total number of threads \(k\) to \(2^sn \leq 2^s\).

\(m\) UTCB size multiplier.
The UTCB location must be aligned to $2^n$. The total size required for one UTCB is $2^n m$.

**Redirector** = nilthread
The current redirector setting for the specified space is not modified.

**Redirector** = anythread
All threads within the specified space are allowed to communicate with any thread in the system.

**Redirector** = anythread, ≠ nilthread
All threads within the specified address space are only allowed to send an IPC to a local thread or to a thread in the same address space as the specified redirector. All other send operations will be deflected to the redirector, the redirected bit (see page 60) in the received message will be set, and the IntendedReceiver TCR will indicate the intended receiver of the message.

**control**
The control field is architecture specific (see Appendix A.5). It is undefined for some architectures, but should for reasons of upward compatibility be set to zero.

**Output Parameters**

**result**
The result is 1 if the operation succeeded completely, 0 otherwise. (The operation may fail because the addressed thread does not exist, and/or the invoker is not sufficiently privileged for the requested operation, and/or the address space contained more than one thread).

**control**
Delivers the space control value that was effective for the thread when the operation was invoked. The value is architecture specific.

**Pagefaults**
No pagefaults will happen.

**Generic Programming Interface**

**System-Call Function:**

```c
#include <l4/space.h>

Word SpaceControl (ThreadId SpaceSpecifier, Word control, Fpage KernelInterfacePageArea, UtcbArea, ThreadId Redirector, Word& old_Control)
```
5.1 Messages And Message Registers (MRs)  [Virtual Registers]

Messages can be sent and received through the IPC system call (see page 57). Basically, the sender writes a message into the sender’s message registers (MRs) and the receiver reads it from the receiver’s MRs. Each thread has 64 MRs, MR_0…63. A message can use some or all MRs to transfer untyped words; it can include memory strings and fpages which are also specified using MRs.

MRs are virtual registers (see page 11), but they are more transient than TCRs. MRs are read-once registers: once an MR has been read, its value is undefined until the MR is written again. The send phase of an IPC implicitly reads all MRs; the receive phase writes the received message into MRs.

The read-once property permits to implement MRs not only by special registers or memory locations, but also by general registers. Writing to such an MR has to block the corresponding general register for code-generator use; reading the MR can release it. Typically, code generated by an IDL compiler will load MRs just before an IPC system call and store them to user variables just afterwards.

Messages

A message consists of up to 3 sections: the mandatory message tag, followed by an optional untyped-words section, followed by an optional typed-items section. The message tag is always held in MR_0. It contains message control information and the message label which can be freely set by the user. The kernel associates no semantics with it. Often, the message label is used to encode a request key or to define the method that should be invoked by the message.

\[
\text{MsgTag [MR}_0\text{]} \begin{array}{cccc}
\text{label (16/48)} & \text{flags (4)} & t (6) & u (6)
\end{array}
\]

\(u\)
Number of untyped words following word 0. MR_1…u hold the untyped words. \(u = 0\) denotes a message without untyped words.

\(t\)
Number of typed-item words following the untyped words or the message tag if no untyped words are present. The typed items use MR_{u+1}…u+t. A message without typed items has \(t = 0\).

\textit{flags}
Message flags, see IPC system call, page 57.

\textit{label}
Freely available, often used to specify the request type or invoked method.

\textit{untyped words [MR}_1…u\text{]}
The optional untyped-words section holds arbitrary data that is untyped from the kernel’s point of view. The data is simply copied to the receiver. The kernel associates no semantics with it.

\textit{typed items [MR}_{u+1}…u+t\text{]}

The optional typed-items section is a sequence of items such as string items (page 52), map items (page 49), and grant items (page 51). Typed message items have their type encoded in the lowermost 4 bits of their first word:

- $0hhC$: StringItem see page 52
- $100C$: MapItem see page 49
- $101C$: GrantItem see page 51
- $110C$: Reserved
- $111C$: Reserved

The $C$ bit signals whether the typed item is followed by another typed item ($C = 1$) or is the last one of the typed-item section ($C = 0$). The typed items must exactly fit into $MR_{u+1...u+t}$.

Note that $C$ and $t$ redundantly describe the message. This is by intention. The $C$ bit allows efficient message parsing, whereas $t + u$ can be used to store all MRs of a message to memory without parsing the complete message. Upon message sending, the $C$ bits are completely ignored. The kernel will, however, ensure that the MRs on the receiver side will have the $C$ bits set properly.

**Example Messages**

**struct (label, Word $[2]$ $w$)**

```
struct (label, Word w [2] w)

    Word $w_2$ (32/64)  MR 2
    Word $w_1$ (32/64)  MR 1

    label (16/48)  flags  $t = 0$  $u = 2$  MR 0
```

**struct (label, MapItem $m$)**

```
struct (label, MapItem m)

    MapItem $m$  1000  MR 1,2

    label (16/48)  flags  $t = 2$  $u = 0$  MR 0
```

**struct (label, Word $w$, StringItem $s_1$, $s_2$)**

```
struct (label, Word w, StringItem s1, s2)

    StringItem $s_2$  0hh0  MR 4,5

    StringItem $s_1$  0hh1  MR 2,3

    Word $w$ (32/64)  MR 1

    label (16/48)  flags  $t = 4$  $u = 1$  MR 0
```

**struct (label, Word $[3]$ $w$, MapItem $m$, GrantItem $g$, StringItem $s$)**
### Generic Programming Interface

The listed generic functions permit user code to access message registers independently of the processor-specific MR model. All functions are user-level functions; the microkernel is not involved.

**MsgTag**

```c
#include <l4/ipc.h>

struct MsgTag { Word raw }

MsgTag NilTag

A message tag with no untyped or typed words, no label, and no flags.

```bool```

```==``` (MsgTag l, r) \[ IsMsgTagEqual \]

```!=``` (MsgTag l, r) \[ IsMsgTagNotEqual \]

Compares all field values of two message tags.

**Word Label** (Msg Tag t)

**Word UntypedWords** (Msg Tag t)

**Word TypedWords** (Msg Tag t)

Delivers the message label, number of untyped words, and number of typed words, respectively.

```MsgTag +``` (MsgTag t, Word label) \[ MsgTagAddLabel \]

```MsgTag +=``` (MsgTag t, Word label) \[ MsgTagAddLabelTo \]

Adds a label to a message tag. Old label information is overwritten by the new label.

**MsgTag MsgTag ()**

**Void Set_MsgTag** (MsgTag t)

Delivers/sets MR₀.
Convenience Programming Interface

IDL-compiler generated Operations

IDL code generators are not restricted to the generic interface for accessing MRs. Instead, they can use processor-specific methods and thus generate heavily optimized code for MR access.

However, such processor-specific MR operations are not generally defined and should be used exclusively by processor-specific IDL code generators. All other programs must use the operations defined in this generic interface.

(Msg

```
#include <4/ipc.h>

struct Msg { Word raw [64] }
```

Void Put (Msg& msg, Word l, int u, Word& [u] ut, int t, {MapItem, GrantItem, StringItem}& Items) [MsgPut]
Loads the specified parameters into the memory object msg. The parameters u and t respectively indicate number of untyped words and number of typed words (i.e., the total size of all typed items). It is assumed that the msg object is large enough to contain all items.

Void Get (Msg& msg, Word& ut, {MapItem, GrantItem, StringItem}& Items) [MsgGet]
Stores the msg object into the specified parameters. Type consistency between the message in the memory object and the specified parameter list is not checked.

(MsgTag(Msg& msg) [MsgMsgTag]
Void Set_MsgTag (Msg& msg, MsgTag t) [Set_MsgMsgTag]
Delivers/sets the message tag of the msg object.

(MsgLabel(Msg& msg) [MsgLabel]
Void Set_Label (Msg& msg, Word label) [Set_MsgLabel]
Delivers/sets the label of the msg object.

Void Load (Msg& msg) [MsgLoad]
Loads message registers MR o... from the msg object.

Void Store (MsgTag t, Msg& msg) [MsgStore]
Stores the message tag t and the current message beginning with MR 1 to the memory object msg. The number of message registers to be stored is derived from t.

Void Clear (Msg& msg) [MsgClear]
Empties the msg object (i.e., clears the message tag).

Void Append (Msg& msg, Word w) [MsgAppendWord]
Void Append (Msg& msg, MapItem m) [MsgAppendMapItem]
Void Append (Msg& msg, GrantItem g) [MsgAppendGrantItem]
Void Append (Msg& msg, StringItem s) [MsgAppendSimpleStringItem]
Void Append (Msg& msg, StringItem& s) [MsgAppendStringItem]
Appends an untyped or a typed item to the msg object. Compound strings must always be passed in by reference. A compound string passed by value will be treated as a simple string (see page 52). It is assumed that there is enough memory in the msg object to contain the new item.

Void Put (Msg& msg, Word u, Word w) [PutWord]
Puts an untyped word at untyped word position u (first untyped word has position 0) in the msg object. It is assumed that the object contains at least u + 1 untyped words.

Void Put (Msg& msg, Word t, MapItem m) [MsgPutMapItem]
**MESSAGES AND MESSAGE REGISTERS (MRS)**

Void **Put** (Msg& msg, Word t, GrantItem g) \[MsgPutGrantItem]\n
Void **Put** (Msg& msg, Word t, StringItem s) \[MsgPutStringItem]\n
Void **Put** (Msg& msg, Word t, StringItem& s) \[MsgPutStringItem]\n
Puts a typed item into the msg object, starting at typed word position t (first typed word has position 0). Compound strings must always be passed in by reference. A compound string passed by value will be treated as a simple string (see page 52). It is assumed that that the object has enough typed words to contain the new item.

Word **Get** (Msg& msg, Word u) \[MsgWord]\n
Void **Get** (Msg& msg, Word u, Word& w) \[MsgGetWord]\n
Delivers the untyped words at position u. It is assumed that the object contains at least u + 1 untyped words.

Word **Get** (Msg& msg, Word t, MapItem& m) \[MsgGetMapItem]\n
Word **Get** (Msg& msg, Word t, GrantItem& g) \[MsgGetGrantItem]\n
Word **Get** (Msg& msg, Word t, StringItem& s) \[MsgGetStringItem]\n
Delivers the typed item starting at typed word position t. It is assumed that the requested item is of the right size and type. Returns the size (in words) of the delivered item.

---

**Low-Level MR Access**

#include "l4/ipc.h"

Void **StoreMR** (int i, Word& w)\n
Void **LoadMR** (int i, Word w)\n
Delivers/sets MR i.

Void **StoreMRs** (int i, k, Word& [k] w)\n
Void **LoadMRs** (int i, k, Word& [k] w)\n
Stores/loads MR i...i+k-1 to/from memory.
5.2 MapItem  [Data Type]

An fpage (see page 36) or IO fpage that should be mapped is sent to the mappee as part of a message. A map operation is a no-op within the same address space. The fpage is specified by a two-word descriptor:

<table>
<thead>
<tr>
<th>snd fpage (28/60)</th>
<th>0 r w x</th>
<th>MR _i+1</th>
</tr>
</thead>
<tbody>
<tr>
<td>snd base / 1024 (22/54)</td>
<td>0 (6)</td>
<td>1 0 0 C</td>
</tr>
</tbody>
</table>

**access rights rwx** The effective access rights for the newly mapped page are calculated by bitwise AND-ing the access rights specified in the snd fpage and the access rights that the mapper itself has on that fpage. As such, the mapper can restrict the effective access rights but not widen them.

**snd base**

The send base specifies the semantics of the map operation if the size of the snd fpage is larger or smaller than the window in which the receiver is willing to accept a mapping (see page 55). If the size of the snd fpage, 2^s, is larger than the receive window, 2^r, the send base indicates which region of the snd fpage that is transmitted. More precisely:

\[
\text{send region} = fpage(\text{addr}_s + 2^s k, 2^r), \text{ for some } k \geq 0 : \\
\text{addr}_s + 2^s k \leq \text{addr}_s + (\text{snd base mod } 2^s) < \text{addr}_s + 2^s k + 2^r
\]

and where \text{addr}_s is the base address of the snd fpage. If the size of the snd fpage, 2^s, is smaller than the receive window, 2^r, the send base indicates where in the receive window the snd fpage is mapped. More precisely:

\[
\text{receive region} = fpage(\text{addr}_r + 2^s k, 2^r), \text{ for some } k \geq 0 : \\
\text{addr}_r + 2^s k \leq \text{addr}_r + (\text{snd base mod } 2^s) < \text{addr}_r + 2^s k + 2^r
\]

and where \text{addr}_r is the base address of the receive window.

Pages already mapped in the mappee’s address space that would conflict with new mappings are implicitly unmapped before new pages are mapped. For performance reasons extension of access rights is possible without prior unmapping, iff the very same mapping already exists. This is the case, when

- the mapper maps from the same address space as the existing mapping; and
- the mapper maps from the same virtual source address as the existing mapping; and
- the mapper maps to the same virtual destination address as the existing mapping; and
- the object (physical address) is the same as the existing mapping.

Access rights can not be revoked by mapping. The access rights of the resulting mapping are a bitwise OR of the existing and the new mapping’s access rights. Access rights are not extended recursively.

---

**Generic Programming Interface**

```c
#include <l4/ipc.h>

struct MAPITEM { Word raw[2] }

MapItem MapItem (Fpage f, Word SndBase)  
    Delivers a map item with the specified fpage and send base.
```
bool MapItem (MapItem m)

Delivers true if map item is valid. Otherwise delivers false.

Fpage SndFpage (MapItem m)

Word SndBase (MapItem m)

Delivers fpage/send base of map item.
5.3 GrantItem [Data Type]

An fpage (see page 36) or IO fpage that should be granted is sent to the mappee as part of a message. It is specified by a two-word descriptor:

\[
\begin{array}{c|c|c}
\text{snd fpage} & \text{0 r w x} & \text{MR} i+1 \\
\hline
\text{snd base / 1024} & \text{0 (6)} & \text{1 0 1 C} \\
\end{array}
\]

access rights \text{rwx} The effective access rights for the granted page are calculated by bitwise anding the access rights specified in the snd fpage and the access rights that the mapper itself has on that fpage. As such, the granter can restrict the effective access rights but not widen them.

snd base The send base specifies the semantics of the map operation if the size of the snd fpage is larger or smaller than the window in which the receiver is willing to accept a mapping (see page 55). If the size of the snd fpage, \(2^s\), is larger than the receive window, \(2^r\), the send base indicates which region of the snd fpage that is transmitted. More precisely:

\[
\text{send region} = \text{fpage} (\text{addr}_s + 2^r k, 2^r), \text{ for some } k \geq 0:
\]

\[
\text{addr}_s + 2^r k \leq \text{addr}_s + (\text{snd base mod } 2^r) < \text{addr}_s + 2^r k + 2^r
\]

and where \(\text{addr}_s\) is the base address of the snd fpage. If the size of the snd fpage, \(2^s\), is smaller than the receive window, \(2^r\), the send base indicates where in the receive window the snd fpage is mapped. More precisely:

\[
\text{receive region} = \text{fpage} (\text{addr}_r + 2^s k, 2^s), \text{ for some } k \geq 0:
\]

\[
\text{addr}_r + 2^s k \leq \text{addr}_r + (\text{snd base mod } 2^s) < \text{addr}_r + 2^s k + 2^s
\]

and where \(\text{addr}_r\) is the base address of the receive window.

Pages already mapped in the grantee’s address space that would conflict with new mappings are implicitly unmapped before new pages are mapped.

---

**Generic Programming Interface**

```
#include <l4/ipc.h>

struct GRANTITEM { Word raw[2] }

GrantItem GrantItem (Fpage f, Word SndBase)
Delivers a grant item with the specified fpage and send base.

bool GrantItem (GrantItem g) [IsGrantItem]
Delivers true if grant item is valid. Otherwise delivers false.

Fpage SndFpage (GrantItem g) [GrantItemSndFpage]
Delivers fpage/send base of grant item.

Word SndBase (GrantItem g) [GrantItemSndBase]
```
5.4 StringItem [Data Type]

A string item specifies a sequence of bytes in user space. No alignment is required, the maximal string size is 4 MB. In send messages, such a string is copied to the receiver buffer when transferring the message. String items are also used to specify receive buffers in buffer registers on the receiver’s side.

**Simple String**

A simple string is a contiguous sequence of bytes.

<table>
<thead>
<tr>
<th>string ptr ( (32/64) )</th>
<th>MR(_{i+1} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>string length ( (22/54) )</td>
<td>0 ( (5) ) 0 ( hh C )</td>
</tr>
</tbody>
</table>

- **string ptr**
  The start address of the string to be sent or the start address of the buffer for receiving a string (no alignment restrictions). However, the string/buffer must fit entirely into the legally addressable user space.

- **string length**
  The length of the string to be sent or the size of the receive buffer. In the second case, strings up to (including) this length can be received. Maximum string length is 4 M bytes, even if the according field is 54 bits wide on 64-bit processors.

- **\( hh \)**
  Cacheability hint. Except for \( hh = 00 \), the semantics of this parameter depends on the processor type (see Appendices A.6 and B.5).

- **\( hh = 00 \)**
  Use the processor’s default cacheability strategy. Typically, cache lines are allocated for data read and written (assuming that the processor’s default strategy is write-back and write-allocate).

**Compound String**

A compound string is a noncontiguous string that consists of multiple contiguous substrings which can be scattered around the entire user address space. The substrings must not overlap. For send and receive IPC operations, a compound string is handled as a single logical string. When sending such a string through IPC, the substrings are transferred as if they were one contiguous string (gather). On the receiver side, a compound string buffer is treated as one logical buffer. The corresponding received string is scattered among the compound buffer’s substrings.

A compound string can be specified as a sequence of substrings where each substring has the form of a simple string except that the continuation flag \( c \) is set for all but the last substring. If \( j \) subsequent substrings have the same size, e.g., for equally sized buffers, a single length word can be used for all \( j \) substrings so that only \( j + 1 \) words instead of \( 2j \) words are required.

<table>
<thead>
<tr>
<th>length word</th>
<th>substring length ( (22/54) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( j ) ( (5) ) ( 0 hh C )</td>
<td></td>
</tr>
</tbody>
</table>

- **\( j \)**
  Number of subsequent string-ptr words. These string ptrs specify \( j \) substrings that have all the same substring length.

- **\( c = 0 \)**
  Continuation flag reset. The compound string descriptor ends with the \( j^\text{th} \) string ptr word following the current length word.

- **\( c = 1 \)**
  Continuation flag set. The current length word and \( j \) string-ptr words are followed by (at least) one substring descriptor, i.e., another length word, etc.
Generic Programming Interface

```c
#include <l4/ipc.h>

struct STRINGITEM { Word raw[*] }

bool StringItem (StringItem& s) [IsStringItem]
Delivers true if string item is valid. Otherwise delivers false.

bool CompoundString (StringItem& s)
Delivers the c-flag value (true = set).

Word Substrings (StringItem& s)

Void* Substring (StringItem& s, Word n)
Delivers number of substrings/address of nth substring.

StringItem StringItem (int size, Void* address)
Delivers a simple string item with the specified size and location.

StringItem & += (StringItem& dest, StringItem AdditionalSubstring) [AddSubstringTo]
Append substring to the string item. It is assumed that there is enough memory in the string item to contain the new substring.

StringItem & += (StringItem& dest, Void* AdditionalSubstringAddress) [AddSubstringAddressTo]
Append a new substring pointer to the string item. It is assumed that there is enough memory in the string item to contain the new substring pointer.
```

Convenience Programming Interface

Support Functions:

```c
#include <l4/ipc.h>

struct CACHE_ALLOCATION_HINT { Word raw }

CacheAllocationHint UseDefaultCacheLineAllocation
```
bool == (CacheAllocationHint l, r)  
   [IsCacheAllocationHintEqual]

bool != (CacheAllocationHint l, r)  
   [IsCacheAllocationHintNotEqual]

Compares two cache allocation hints.

CacheAllocationHint CacheAllocationHint (StringItem s)  
   Delivers the cache allocation hint of the string item.

StringItem + (StringItem s, CacheAllocationHint h)  
   [AddCacheAllocationHint]

StringItem += (StringItem s, CacheAllocationHint h)  
   [AddCacheAllocationHintTo]
   Adds a cache allocation hint to a string item. An already existing hint is overwritten.
5.5 String Buffers And Buffer Registers (BRs)  [Pseudo Registers]

For receiving messages that contain string items, the receiver has to specify appropriate string buffers. Such buffers are described by string items (see page 52). A buffer can be contiguous (simple string) or non-contiguous (compound string).

Such buffer descriptors are held in 34 per-thread Buffer Registers BR[0...33]. The number of buffer registers is sufficient to specify, for example, one compound buffer of 32 equally-sized sub-buffers. Up to 16 buffers can be specified provided that not more than 34 BRs are required.

When a message is received, the first message string item is copied into the first buffer string item which starts at BR[1]; the next message string item is copied to the next buffer string item, etc. The list of buffer strings is terminated by having the C bit in the item type specifier of the last string zeroed.

BRs are registers in the sense that they are per-thread objects and can only be addressed directly, not indirectly through pointers. BRs are static objects like TCRs, i.e., they keep their values until explicitly modified. BRs can be mapped to either special registers or to memory locations.

---

**Acceptor** [BR[0]]

RcvWindow (28/60) 0 0 0 0

BR[0] specifies which typed items are accepted when a message is received.

**RcvWindow**

Fpage (without access bits) that specifies the address-space window in which mappings and grants are accepted. Nilpage denies any mapping or granting; CompleteAddressSpace accepts any mapping or granting.

**s**

StringItems are accepted iff s = 1.

---

**buffer string items** [BR[1]...]

contain the valid buffer string items. Ignored if s = 0 in BR[0].

---

**Generic Programming Interface**

The listed generic functions permit user code to access buffer registers independently of the processor-specific BR model. All functions are user-level functions; the microkernel is not involved.

**Acceptor**

```c
#include <l4/ipc.h>

struct Acceptor { Word raw }

Acceptor UntypedWordsAcceptor
Acceptor StringItemsAcceptor
Acceptor MapGrantItems (Fpage RcvWindow)
```

Delivers an acceptor which allows untyped words, string items, or mappings and grants.

**Acceptor + (Acceptor l, r)** [AddAcceptor]

**Acceptor += (Acceptor l, r)** [AddAcceptorTo]

Adds mappings/grants or string items to an acceptor. Adding a non-nil receive window will replace an existing window.

**Acceptor – (Acceptor l, r)** [RemoveAcceptor]

**Acceptor -= (Acceptor l, r)** [RemoveAcceptorFrom]

Removes mappings/grants or string items from an acceptor. Removing a non-nil receive window will deny all mappings or grants, regardless of the size of the receive window.
bool StringItems (Acceptor a)  
\[\text{HasStringItems}\]
Checks whether string items/mappings are allowed.

bool MapGrantItems (Acceptor a)  
\[\text{HasMapGrantItems}\]

Fpage RcvWindow (Acceptor a)  
Delivers the address space window where mappings and grants are accepted. Delivers nilpage if mappings or grants are not allowed.

Void Accept (Acceptor a)  
Sets BR\textsubscript{0}.

Void Accept (Acceptor a, MsgBuffer\& b)  
\[\text{AcceptStrings}\]
Sets BR\textsubscript{0} and loads the buffer description \(b\) into BR\textsubscript{1}.

Acceptor Accepted ()  
Delivers BR\textsubscript{0}.

---

**Convenience Programming Interface**

**MsgBuffer**

\[
\text{#include } \langle l4/ipc.h\rangle
\]

struct MSGBUFFER { Word raw[32] }

Void Clear (MsgBuffer\& b)  
\[\text{MsgBufferClear}\]
Clears the message buffer (i.e., inserts a single empty string into it).

Void Append (MsgBuffer\& b, StringItem s)  
\[\text{MsgBufferAppendSimpleRcvString}\]

Void Append (MsgBuffer\& b, StringItem * s)  
\[\text{MsgBufferAppendRcvString}\]
Appends a string buffer to the message buffer. Compound strings must always be passed in by reference. A compound string passed by value will be treated as a simple string. It is assumed that there is enough memory in the message buffer object to contain the new string buffer.

---

**Low-Level BR Access**

\[
\text{#include } \langle l4/ipc.h\rangle
\]

Void StoreBR (int i, Word\& w)  

Void LoadBR (int i, Word w)  
Delivers/sets the value of BR\textsubscript{i}.

Void StoreBRs (int i, k, Word\& [k])

Void LoadBRs (int i, k, Word\& [k])  
Stores/loads BR\textsubscript{i...i+k-1} to/from memory.

---

Code generators of IDL and other compilers are not restricted to the generic interface. They can use any processor-specific methods and optimizations to access BRs.
5.6 IPC [Systemcall]

IPC is the fundamental operation for inter-process communication and synchronization. It can be used for intra- and inter-address-space communication. All communication is synchronous and unbuffered: a message is transferred from the sender to the recipient if and only if the recipient has invoked a corresponding IPC operation. The sender blocks until this happens or until a period specified by the sender has elapsed without the destination becoming ready to receive.

IPC can be used to copy data as well as to map or grant fpages from the sender to the recipient. For the description of messages see page 44. A single IPC call combines an optional send phase and an optional receive phase. Which phases are included is determined by the parameters to and FromSpecifier. Transitions between send phase and receive phase are atomic.

IPC operations are also controlled by MRs, BRs and some TCRs. RcvTimeout and SndTimeout are directly specified as system-call parameters. Each timeout can be 0, ∞ (i.e., never expire), relative or absolute. For details on timeouts see page 28.

Variants

To enable implementation-specific optimizations, there exist two variants of the IPC system call. Functionally, both variants are identical. Transparently to the user, a kernel implementation can unify both variants or implement differently optimized functions.

| IPC | Default IPC function. Must always be used except if all criteria for using LIPC are fulfilled. |
| LIPC | IPC function that may be optimized for sending messages to local threads. Should be used whenever it is absolutely clear that in the overwhelming majority of all invocations |
|     | • a send phase is included; and |
|     | • the destination thread is specified as a local thread ID; and |
|     | • a receive phase is included; and |
|     | • the destination thread runs on the same processor; and |
|     | • the RcvTimeout is ∞, and |
|     | • the IPC includes no map/grant operations. |

Input Parameters

| to = nilthread | IPC includes no send phase. |
| to ≠ nilthread | Destination thread; IPC includes a send phase |

| FromSpecifier = nilthread | IPC includes no receive phase. |
**FromSpecifier = anythread**

IPC includes a receive phase. Incoming messages are accepted from any thread (including hardware interrupts).

**FromSpecifier = anylocalthread**

IPC includes a receive phase. Incoming messages are accepted from any thread that resides in the current address space.

**FromSpecifier ≠ nilthread, ≠ anythread, ≠ anylocalthread**

IPC includes a receive phase. Incoming messages are accepted only from the specified thread. (Note that hardware interrupts can be specified.)

---

<table>
<thead>
<tr>
<th>Timeouts</th>
<th>SndTimeout (16)</th>
<th>RcvTimeout (16)</th>
</tr>
</thead>
</table>

**RcvTimeout**

The receive phase waits until either a message transfer starts or the RcvTimeout expires. Ignored for send-only IPC operations.

For relative receive timeout values, the receive timeout starts to run after the send phase has successfully completed. If the receive timeout expires before the message transfer has been started IPC fails with “receive timeout”. A pending incoming message is received if the timeout period is 0.

**SndTimeout**

If the send timeout expires before the message transfer could start the IPC operation fails with “send timeout”. A send timeout of 0 ensures that IPC happens only if the addressed receiver is ready to receive when the send IPC operation is invoked. Otherwise, IPC fails immediately, i.e., without blocking.

---

<table>
<thead>
<tr>
<th>MsgTag [MR0]</th>
<th>label (16/48)</th>
<th>0 (3)</th>
<th>p</th>
<th>t (6)</th>
<th>u (6)</th>
</tr>
</thead>
</table>

**Message head of the message to be sent.** Only the upper 16/48 bits are freely available. The lower 16 bits hold the SndControl parameter. It describes the message to be sent and contains some control bits; ignored if no send phase.

**u**

Number of untyped words following word 0. MR \(_1...u\) hold the untyped words. \(u = 0\) denotes a message with no untyped words.

**t**

Number of words holding typed items that follow the untyped words (or the message tag if no untyped words are present). The typed items use MR \(_{u+1}\) and following MRs, potentially up to MR \(_{63}\). \(t = 0\) denotes a message without typed items.

\(p=0\)

Normal (unpropagated) send operation. The recipient gets the original sender’s id.

\(p=1\)

Propagating send operation. The VirtualSender TCR specifies the id of the originator thread. (i.e., the thread to send the message on behalf of). If originator thread and current sender, or current sender and receiver reside in the same address space, propagation is always permitted. Otherwise, IPC occurs unpropagated. Propagation is also allowed if the originator thread is an interrupt thread waiting (closed) for the current thread, or if the current sender is a redirector for the originator thread (or there exists a chain of redirectors from the originator to the current sender).

If propagation is permitted, the receiver receives the originator’s id instead of the current sender’s id, the \(p\) bit in the receiver’s MsgTag is set, and the current sender’s id is stored in the receiver’s ActualSender TCR. If the originator thread is waiting (closed) for a reply from the current sender, the originator’s state is additionally modified so that it now waits for the new receiver instead of the current sender.

**label**

Freely available, often used to specify the request type or invoked method, respectively.

\([MR1...u]\)

Untyped words to be sent. Ignored if no send phase.

\([MR_{u+1}...u+t]\)

Typed items to be sent. Ignored if no send phase.
### XferTimeouts [TCR]

Once a message transfer has been started, the time for transferring the message is roughly bounded by the minimum of sender’s and receiver’s XferTimeout. “Roughly” means that xfer timeouts are only checked when message copy raises a pagefault in the sender’s or in the receiver’s address space. Copying data and mapping/granting is assumed to take no time. A relative transfer timeout always refers to the beginning of the message transfer (actually when the first page fault is raised). Logically, at that point it is transferred into an absolute timeout which then is used as send and receive timeout for the first and all subsequent page-fault RPCs in the message transfer.

If the effective transfer timeout expires during the message transfer, IPC fails with “xfer timeout” (on both sides). Additional information specifies whether the page fault was in the receiver’s or in the sender’s address space and which part of the message was already transferred. Each thread has two transfer timeouts. One for the send phase and one for the receive phase.

### Acceptor [BR₀]

<table>
<thead>
<tr>
<th>RevWindow (28/60)</th>
<th>000s</th>
</tr>
</thead>
</table>

BR₀ specifies which typed items are accepted when a message is received.

### RcvWindow

Fpage (without access bits) that specifies the address-space window in which mappings and grants are accepted. Nilpage denies any mapping or granting; CompleteAddressSpace accepts any mapping or granting.

### s

StringItems are accepted iff s = 1.

### Buffer strings [BR₁,...]

contain the valid buffer string items. Ignored if s = 0 in BR₀.

### Output Parameters

#### from

Thread ID of the sender from which the IPC was received. Thread IDs are delivered as local thread IDs iff they identify a thread executing in the same address space as the current thread. It does not matter whether the sender specified the destination as local or global id. Only defined for IPC operations that include a receive phase.

#### MsgTag [MR₀]

<table>
<thead>
<tr>
<th>label (16/48)</th>
<th>E X r p</th>
<th>t (6)</th>
<th>u (6)</th>
</tr>
</thead>
</table>

If the IPC operation included a receive phase, MR₀ contains the message tag of the received message. The upper 16/48 bits contain the user-specified label. The lower bits describe the received message, contain the error indicator, and the cross-processor IPC indicator. **MR₀ is defined even if the IPC operation did not include a receive phase.** In the send-only case, MR₀ returns the error indicator.

u

Number of untyped words following word 0. u = 0 means no untyped words. For IPC operations without receive phase, u = 0 is delivered.

t

Number of received words that hold typed items. t = 0 means no typed items. For IPC operations without receive phase, t = 0 is delivered.

p

Propagated IPC. If reset (p = 0) the IPC was not propagated. If set (p = 1) the IPC was propagated and the FromSpecifier indicates the originator thread’s id. The ActualSender specifies the id of the thread which performed the propagation.
Redirected IPC. If reset ($r = 0$) the IPC was not a redirected one. If set ($r = 1$) the IPC was redirected to the current thread, and the IntendedReceiver TCR specifies the id of the thread supposed to receive the message.

Cross-processor IPC. If reset ($X = 0$) the received IPC came from a thread running on the same processor as the receiver. If set ($X = 1$) the received IPC was cross-processor. For IPC operations without receive phase, $X = 0$ is delivered.

Error indicator. If reset ($E = 0$) the IPC operation terminated successfully. If set ($E = 1$) IPC failed. If the send phase was successful but a receive timeout occurred afterwards, or if a message could only be partially transferred, the entire IPC fails. The error code and additional information can be retrieved from the ErrorCode TCR. The fields label, $t$, and $u$ are valid if the error code signals a partially received message.

Label of the received message. For IPC operations without receive phase, the label is 0.

 Untyped words that have been received. Undefined if no receive phase.

 Typed items that have been received. Undefined if no receive phase.

---

**Error Code [TCR]**

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E$</td>
<td>Error indicator. If reset ($E = 0$) the IPC operation terminated successfully. If set ($E = 1$) IPC failed. If the send phase was successful but a receive timeout occurred afterwards, or if a message could only be partially transferred, the entire IPC fails. The error code and additional information can be retrieved from the ErrorCode TCR. The fields label, $t$, and $u$ are valid if the error code signals a partially received message.</td>
</tr>
<tr>
<td>$p$</td>
<td>Specifies whether the error occurred during the send phase ($p = 0$) or the receive phase ($p = 1$).</td>
</tr>
</tbody>
</table>

**Errors 1, 2, 3**

- $e = 1$: Timeout. 
  - From is undefined in this case.
- $e = 2$: Non-existing partner. If the error occurred in the send phase, to does not exist. (Anythread as a destination is illegal and will also raise this error.) If the error occurred in the receive phase, FromSpecifier does not exist. (FromSpecifier = anythread is legal, and thus will never raise this error.)
- $e = 3$: Canceled by another thread (system call exchange registers).

**Errors 4, 5, 6, 7**

- $e = 4$: Message Overflow. 
  - A message overflow can occur (1) if a receiving buffer string is too short, (2) if not enough buffer string items are present, and (4) if a map/grant of an fpage fails because the system has not enough page-table space available. The offset in conjunction with the received MRs permits sender and receiver to exactly determine the reason.
- $e = 5$: Xfer timeout during page fault in the invoker’s address space.

**Offset**

The message transfer has been started and could not be completed. The offset identifies exactly the number of bytes that have been been transferred successfully so far through string items.
Pagefaul

Three different types of pagefault can occur during ipc: pre-send, post-receive, and xfer pagefaults. Only xfer pagefaults are critical from a security point of view. Fortunately, messages without strings will never raise xfer pagefaults and need thus no special pagefault provisions:

**Pre-send pagefaults** happen in the sender’s context before the message transfer has really started. The destination thread is not involved; in particular, it is not locked. Therefore, the destination thread might receive another message or time out while the sender’s pre-send pagefault is handled. Send and transfer timeouts do not control pre-send pagefaults. Pre-send pagefaults are uncritical from a security point of view since only the sender’s own pager is involved and only the sender could suffer from its potential misbehavior.

**Post-receive pagefaults** happen in the receiver’s context after the message has been transferred. The sender thread is no longer involved, especially, it is no longer locked. Consequently, post-receive pagefault are not subject to send and transfer timeouts. Like pre-send pagefaults, post-receive pagefaults are also uncritical from a security perspective since only the receiver and its pager are involved.

**Xfer pagefaults** happen while the message is being transferred and both sender and receiver are involved. Therefore, xfer pagefaults are critical from a security perspective: If such a pagefault occurs in the receiver’s space, the sender may be starved by a malicious receiver pager. An xfer pagefault in the sender’s space and a malicious sender pager may starve the receiver. As such, xfer pagefaults are controlled by the minimum of sender’s and receiver’s xfer timeouts.

However, xfer pagefaults can only happen when transferring strings. *Send messages without strings or receive buffers without receive string buffers are guaranteed not to raise xfer pagefaults.*

---

**Generic Programming Interface**

**System-Call Function:**

```c
#include <l4/ipc.h>

MsgTag Ipc (ThreadId to, FromSpecifier, Word Timeouts, ThreadId& from)
MsgTag Lipc (ThreadId to, FromSpecifier, Word Timeouts, ThreadId& from)
```

Note that message registers have read-once semantics and that returning the message tag implies reading MR₀. The contents of the message tag is therefore lost if the application does not implicitly store the return value of IPC or LIPC.

---

**Convenience Programming Interface**

**Derived Functions:**

```c
#include <l4/ipc.h>

MsgTag Call (ThreadId to)
    { Call (to, never, never) }
```
MsgTag Call (ThreadId to, Time SndTimeout, RcvTimeout)  
   { Ipc (to, to, Timeouts (SndTimeout, RcvTimeout), –) }  
[Call_Timeouts]

MsgTag Send (ThreadId to)  
   { Send (to, never) }

MsgTag Send (ThreadId to, Time SndTimeout)  
   { Ipc (to, nilthread, Timeouts (SndTimeout, –), –) }

MsgTag Reply (ThreadId to)  
   { Send (to, ZeroTime) }

MsgTag Receive (ThreadId from)  
   { Receive (from, never) }

MsgTag Receive (ThreadId from, Time RcvTimeout)  
   { Ipc (nilthread, from, Timeouts (–, RcvTimeout), –) }

MsgTag Wait (ThreadId& from)  
   { Wait (never, from) }

MsgTag Wait (Time RcvTimeout, ThreadId& from)  
   { Ipc (nilthread, anythread, Timeouts (–, RcvTimeout), from) }

MsgTag ReplyWait (ThreadId to, ThreadId& from)  
   { ReplyWait (to, never, from) }

MsgTag ReplyWait (ThreadId to, Time RcvTimeout, ThreadId& from)  
   { Ipc (to, anythread, Timeouts (TimePeriod(0), RcvTimeout), from) }

Void Sleep (Time t)  
   { Set_MsgTag (Receive (MyLocalId, t)) }

MsgTag Lcall (ThreadId to)  
   { Lipc (to, to, Timeouts (never, never), –) }

MsgTag LreplyWait (ThreadId to, ThreadId& from)  
   { Lipc (to, anylocalthread, Timeouts (TimePeriod(0), never), from) }

---

Support Functions:

#include <l4/ipc.h>

bool IpcSucceeded (Msg Tag t)  
bool IpcFailed (Msg Tag t)
   Deliveres the state of the error indicator (the \( E \) bit of MR\(_0\)).

bool IpcPropagated (Msg Tag t)  
bool IpcRedirected (Msg Tag t)  
bool IpcXcpu (Msg Tag t)
   Checks if the IPC was propagated/redirected/cross cpu.

Word ErrorCode ()
ThreadId IntendedReceiver ()
Threadid ActualSender ()
    Delivers the error code/intended receiver TCR/actual sender.

Void SetPropagation (Msg & Tag t)
    Sets the propagation bit.

Void SetVirtualSender (ThreadId t)
    Sets the virtual sender TCR.

Word Timeouts (Time SndTimeout, RcvTimeout)
    Delivers a word containing both timeout values.
Chapter 6

Miscellaneous
### 6.1 ExceptionHandler [TCR]

An exception handler thread can be installed to receive exception IPCs.

#### ExceptionHandler

- \#nilthread: specifies the exception handler thread. When a thread raises an exception the kernel sends an exception IPC message on the thread’s behalf to the thread’s exception handler thread and waits for a response from the exception handler containing the instruction pointer where the thread should continue execution in MR 1. The format of the exception IPC message is architecture specific. The architectural registers of the faulting thread, BR 0, TCRs, and the MRs containing the exception message are preserved.

- =nilthread: No exception handler is specified. If an exception is raised the thread is halted and not scheduled anymore. \textit{nilthread is the default value for newly created threads.}

#### Generic Programming Interface

```c
#include <l4/thread.h>

ThreadId ExceptionHandler ()

Void SetExceptionHandler (ThreadId new)
    Delivers/sets the exception handler TCR.
```
6.2 Cop Flags [TCR]

The coprocessor flags TCR helps the kernel to optimize thread switching for some hardware architectures.

\[
\begin{array}{c}
C_7 \ldots C_0 \\
\end{array}
\]

By resetting a \( C_i \)-bit to 0, a thread tells the system that it no longer needs coprocessor \( i \). If the kernel finds \( C_i = 0 \), it concludes that registers and state of coprocessor \( i \) do not have to be saved. However, the kernel ensures that the coprocessor can not be used as a covert channel between different address spaces.

Once a thread has reset bit \( C_i \) it must set \( C_i \) to 1 before it issues the next operation on coprocessor \( i \). Otherwise, coprocessor registers and state might be arbitrarily modified while using it.

Note that the \( C_i \)-bits are write-only. Reading them results in an undefined value. Upon thread creation, all \( C_i \)-bits are set to 1.

**Generic Programming Interface**

\begin{verbatim}
#include <l4/thread.h>

Void Set_CopFlag (Word n)

Void Clr_CopFlag (Word n)

Sets/clears coprocessor flag \( C_n \).
\end{verbatim}
### 6.3 ProcessorControl

[Privileged Systemcall]

<table>
<thead>
<tr>
<th>Word</th>
<th>ProcessorNo</th>
<th>→</th>
<th>Word</th>
<th>result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Word</td>
<td>InternalFrequency</td>
<td></td>
<td>Word</td>
<td>ExternalFrequency</td>
</tr>
<tr>
<td>Word</td>
<td>voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Control the internal frequency, external frequency, or voltage for a system processor.

#### Input Parameters

**ProcessorNo**

Specifies the processor to control. Number must be a valid index into the processor descriptor array (see Kernel Interface Page, page 4).

All further input parameters have no effect if the supplied value is $-1$, ensuring that the corresponding value is not modified. The following description always refers to values $\neq -1$.

**InternalFrequency**

Sets internal frequency for processor to the given value (in kHz).

**ExternalFrequency**

Sets external frequency for processor to the given value (in kHz).

**voltage**

Sets voltage for processor to the given value (in mV). A value of 0 shuts down the processor.

#### Output Parameters

**result**

The result is 1 if the operation succeeded completely, 0 otherwise. (The operation may fail because the specified processor number is invalid or the invoker is not sufficiently privileged for the requested operation.)

Note that the active internal and external frequency of all processors are available to all threads via the kernel interface page.

#### Pagefaults

No pagefaults will happen.

#### Generic Programming Interface

**System-Call Function:**

```c
#include <l4/misc.h>
```
Word ProcessorControl (Word ProcessorNo, control, InternalFrequency, ExternalFrequency, voltage)
6.4 MEMORYCONTROL  [Privileged Systemcall]

\[
\begin{align*}
\text{Word} & \quad \text{control} & \rightarrow & \text{Void} \\
\text{Word} & \quad \text{attribute}_0 \\
\text{Word} & \quad \text{attribute}_1 \\
\text{Word} & \quad \text{attribute}_2 \\
\text{Word} & \quad \text{attribute}_3
\end{align*}
\]

Set the page attributes of the fpages (MR \(_{0...k}\)) to the \text{attribute} specified with the fpage.

---

**Input Parameters**

- \(\text{control} \): 0 (26/58) \(k\) (6)

\(k\): Specifies the highest MR \(_k\) that holds an fpage to set the attributes. The number of fpages is thus \(k + 1\).

- \(\text{attribute}_i\): Specifies the attribute to associate with an fpage. The semantics of the \(\text{attribute}_i\) values are hardware specific, except for the value 0 which specifies default semantics.

- \(\text{FpageList MR}_{0...k}\): Fpages to be processed.

- \(\text{Fpage MR}_a\): Fpage to change the attributes. A nilpage specifies a no-op.

- \(\alpha\): selects \(\text{attribute}_\alpha\) to be set as the fpages memory attributes.

---

**Pagefaults**

No pagefaults will happen.

---

**Generic Programming Interface**

**System-Call Function:**

```c
#include <l4/misc.h>

\text{Void MemoryControl} (\text{Word control, Word& attributes[4]})
```

```c
\text{Word DefaultMemory}
```
Convenience Programming Interface

Derived Functions:

```c
#include <l4/misc.h>

Void Set_PageAttribute (Fpage f, Word attribute)
{ LoadMR (0, f); MemoryControl (0, &attribute); }

{ LoadMRs (0, n, fpages); MemoryControl (n − 1, attributes); }
```
Chapter 7

Protocols
7.1 Thread Start Protocol

Newly created active threads start immediately by receiving a message from its pager. The received message contains the initial instruction-pointer and stack-pointer for the thread.

<table>
<thead>
<tr>
<th>From Pager</th>
<th>Initial SP (32/64)</th>
<th>MR 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial IP (32/64)</td>
<td>0 (16/48)</td>
<td>0 (4)</td>
</tr>
<tr>
<td></td>
<td>t = 0 (6)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>u = 2 (6)</td>
<td></td>
</tr>
<tr>
<td>MR 0</td>
<td>0 (16/48)</td>
<td>0 (4)</td>
</tr>
<tr>
<td>MR 1</td>
<td>t = 0 (6)</td>
<td></td>
</tr>
<tr>
<td>MR 2</td>
<td>u = 2 (6)</td>
<td></td>
</tr>
</tbody>
</table>
7.2 Interrupt Protocol

Interrupts are delivered as an IPC call to the interrupt handler thread (i.e., the pager of the interrupt thread). The interrupt is disabled until the interrupt handler sends a re-enable message.

**From Interrupt Thread**

\[
\begin{array}{cccc}
-1_{(12/44)} & 0_{(4)} & t = 0_{(6)} & u = 0_{(6)} \\
\end{array}
\]

**To Interrupt Thread**

\[
\begin{array}{cccc}
0_{(16/48)} & 0_{(4)} & t = 0_{(6)} & u = 0_{(6)} \\
\end{array}
\]
7.3 Pagefault Protocol

A thread generating a pagefault will cause the kernel to transparently generate a pagefault IPC to the faulting thread’s pager. The behavior of the faulting thread is undefined if the pager does not exactly follow this protocol.

<table>
<thead>
<tr>
<th>To Pager</th>
<th>MR 2</th>
<th>MR 1</th>
<th>MR 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>faulting user-level IP</td>
<td>fault address</td>
<td>rwx</td>
<td>0/rwx</td>
</tr>
<tr>
<td>(32/64)</td>
<td>(32/64)</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

The `rwx` bits specify the fault reason:

- `r` read fault
- `w` write fault
- `x` execute fault

A bit set to one reports the type of the attempted access. On processors that do not differentiate between read and execute accesses, `x` is never set. Read and execute accesses will both be reported by the `r` bit.

<table>
<thead>
<tr>
<th>Acceptor [BR0]</th>
<th>BR 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (22/54)</td>
<td>s = 1</td>
</tr>
</tbody>
</table>

The acceptor covers the complete user address space. The kernel accepts mappings or grants into this region on behalf of the faulting thread. The received message is discarded.

<table>
<thead>
<tr>
<th>From Pager</th>
<th>MR 1,2</th>
<th>MR 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MapItem / GrantItem</td>
<td>0 (16/48)</td>
<td>0 (4)</td>
</tr>
</tbody>
</table>

|             | 6 | 6 | 6 | 6 |
7.4 Preemption Protocol

From Preempted Thread

<table>
<thead>
<tr>
<th></th>
<th>MR₂</th>
<th>MR₁</th>
<th>MR₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock (\frac{32}{64}) (\frac{32}{64})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock mod(\frac{32}{64}) (\frac{32}{64})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(-3) (\frac{12}{44})</td>
<td>0 (4)</td>
<td>0 (4)</td>
<td>(t = 0) (6)</td>
</tr>
</tbody>
</table>

The preemption message contains the system clock when the thread was preempted. The preemption message is sent with relative timeout 0. If the message cannot be delivered (e.g., due to timeouts) the message is dropped.
### 7.5 Exception Protocol

The exception IPC contains a label, the faulting instruction pointer, and additional architecture specific exception words. The reply from the exception handler contains a label, an instruction pointer where the faulting thread is resumed, and an optional number of additional architecture specific words.

Note that the stack pointer is not explicitly specified to allow architecture specific optimizations.

#### To Exception Handler

<table>
<thead>
<tr>
<th>exception word (k - 1) (32/64)</th>
<th>MR (k + 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>exception word (0) (32/64)</td>
<td>MR 2</td>
</tr>
<tr>
<td>IP (32/64)</td>
<td>MR 1</td>
</tr>
<tr>
<td>label (12/44)</td>
<td>0 (4)</td>
</tr>
<tr>
<td></td>
<td>0 (4)</td>
</tr>
<tr>
<td></td>
<td>(t = 0)</td>
</tr>
<tr>
<td></td>
<td>(u = k)</td>
</tr>
</tbody>
</table>

\(k\) Number of exception words.

\(label\) specifies the exception type.

\(-4\) System exceptions are defined for all architectures.

\(-5\) Architecture specific exceptions.

#### From Exception Handler

<table>
<thead>
<tr>
<th>exception reply word (k - 1) (32/64)</th>
<th>MR (k + 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>exception reply word (0) (32/64)</td>
<td>MR 2</td>
</tr>
<tr>
<td>IP (32/64)</td>
<td>MR 1</td>
</tr>
<tr>
<td>0 (16/48)</td>
<td>0 (4)</td>
</tr>
<tr>
<td>(t = 0)</td>
<td>(u = k)</td>
</tr>
</tbody>
</table>

\(k\) Number of exception reply words.

\(IP\) Location where execution is resumed in the faulting thread.
7.6 Sigma0 RPC protocol  [Protocol]

\( \sigma_0 \) is the initial address space. Although it is not part of the kernel, its basic protocol is defined with the kernel. Specific \( \sigma_0 \) implementations may extend this protocol.

The address space \( \sigma_0 \) is idempotent, i.e., all virtual addresses in this address space are identical to the corresponding physical address. Note that pages requested from \( \sigma_0 \) continue to be mapped idempotently if the receiver specifies its complete address space as receive fpage.

\( \sigma_0 \) gives pages to the kernel and to arbitrary tasks, but only once. The idea is that all pagers request the memory they need in the startup phase of the system so that afterwards \( \sigma_0 \) has exhausted all its memory. Further requests will then automatically be denied.

### Kernel Protocol

**To \( \sigma_0 \)**

<table>
<thead>
<tr>
<th>Requested fpage</th>
<th>MR 2</th>
<th>MR 1</th>
<th>MR 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>( -6_{(12/44)} )</td>
<td>0 (4)</td>
<td>0 (4)</td>
<td>( t = 0 ) (6)</td>
</tr>
</tbody>
</table>

**Requested fpage**

\( s = 0 \) Kernel requests the amount of memory recommended by \( \sigma_0 \) for kernel use (pagetable and other kernel-internal data).

\( s \neq 0 \) Kernel requests an fpage of size \( 2^s \). The fpage can be located at an arbitrary position but must contain ordinary memory. If a free fpage of size \( 2^s \) is available, it is granted to the kernel.

**rwx** The \( rwx \) bits are ignored. \( \sigma_0 \) always grants fpages with maximum access rights to the kernel.

### From \( \sigma_0 \)

**Kernel memory recommendation**

<table>
<thead>
<tr>
<th>Amount</th>
<th>MR 2</th>
<th>MR 1</th>
<th>MR 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 0_{(32/64)} )</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Amount** Amount of memory recommended for kernel use (in bytes).

**Grant Response**

<table>
<thead>
<tr>
<th>GrantItem</th>
<th>MR 1,2</th>
<th>MR 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 0_{(16/48)} )</td>
<td>( 0_{(4)} )</td>
<td>( t = 2 ) (6)</td>
</tr>
</tbody>
</table>
Grant Reject

User Protocol

To $\sigma_0$

Requested attributes (32/64)

Requested fpage (32/64)

Requested fpage $b/2^s$ (22/54)

The $rwx$ bits are ignored. $\sigma_0$ always maps fpages with maximum access rights to the requestor.

Requested attributes

$= 0$ The page is requested with default attributes.

$\neq 0$ The page is requested with some architecture dependent attributes.

From $\sigma_0$

Map Response

The page is mapped to the requesting thread's address space and marked as owned by the requesting thread. No new mapping operations happen.
$\sigma_0$ responds with a *map reject* message if the page is reserved (i.e., kernel space) or already mapped to a different thread, or if memory is exhausted.

<table>
<thead>
<tr>
<th>Map Reject</th>
<th>nilpage (32/64)</th>
<th>0 (28/60)</th>
<th>1 0 0 0</th>
<th>0 (16/48)</th>
<th>0 (4)</th>
<th>t = 2 (6)</th>
<th>u = 0 (6)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MR_2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MR_1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MR_0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
7.7 Generic Booting  [Protocol]

Machine-specific boot procedures are described on pages 99 ff.

After booting, L4 initializes itself. It generates the basic address space-servers $\sigma_0$, $\sigma_1$ and a root server which is intended to boot the higher-level system. $\sigma_0$, $\sigma_1$ and the root server are user-level servers and not part of the pure kernel. The predefined ones can be replaced by modifying the following table in the L4 image before starting L4. An empty area specifies that the corresponding server should not be started. Note, that $\sigma_0$ is a mandatory service. The kernel debugger $kdebug$ is also not part of the kernel and can accordingly be replaced by modifying the table.

<table>
<thead>
<tr>
<th>MemoryDesc</th>
<th>MemDescPtr</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\sim$</td>
<td>$\sim$</td>
</tr>
<tr>
<td>$\sim$</td>
<td>$\sim$</td>
</tr>
<tr>
<td>$\sim$</td>
<td>$\sim$</td>
</tr>
<tr>
<td>$\sim$</td>
<td>$\sim$</td>
</tr>
<tr>
<td>$\sim$</td>
<td>$\sim$</td>
</tr>
<tr>
<td>$\sim$</td>
<td>$\sim$</td>
</tr>
<tr>
<td>$\sim$</td>
<td>$\sim$</td>
</tr>
<tr>
<td>$\sim$</td>
<td>$\sim$</td>
</tr>
<tr>
<td>$\sim$</td>
<td>$\sim$</td>
</tr>
</tbody>
</table>

The addresses are offsets relative to the configuration page’s base address. The configuration page is located at a page boundary and can be found by searching for the magic “L4µK” starting at the load address. The IP and SP values however, are absolute addresses. The appropriate code must be loaded at these addresses before L4 is started.

**IP**

Physical address of a server’s initial instruction pointer (start).

**SP**

Physical address of a server’s initial stack pointer (stack bottom).

**Kdebug.init**

Physical address of $kdebug$’s initialization routine.
**Kdebug.entry**
Physical address of *kdebug*’s exception handler entry point.

**Kdebug.low**
Physical address of first byte of kernel debugger. Must be page aligned.

**Kdebug.high**
Physical address of last byte of kernel debugger. Must be the last byte in page.

**Kdebug.config**
Configuration fields which can be freely interpreted by the kernel debugger. The specific semantics of these fields are provided with the specific kernel debuggers.

**BootInfo**
Prior to kernel initialization a boot loader can write an arbitrary value into this field. Post-initialization code, e.g., a root server can later read the field. Its value is neither changed nor interpreted by the kernel. This is the generic method for passing system information across kernel initialization.

**MemoryInfo**

<table>
<thead>
<tr>
<th>MemDescPtr (16/32)</th>
<th>n (16/32)</th>
</tr>
</thead>
</table>

**MemDescPtr**
Location of first memory descriptor (as an offset relative to the configuration page’s base address). Subsequent memory descriptors are located directly following the first one. For memory descriptors that specify overlapping memory regions, later descriptors take precedence over earlier ones.

**n**
Initially equals the number of available memory descriptors in the configuration page. Before starting L4 this number must be initialized to the number of inserted memory descriptors.

**MemoryDesc**

<table>
<thead>
<tr>
<th>high/2(^{20}) (22/54)</th>
<th>~ (10)</th>
<th>low/2(^{10}) (22/54)</th>
<th>t (4)</th>
<th>type (4)</th>
</tr>
</thead>
</table>

Memory descriptors should be initialized before starting L4. The kernel may after startup insert additional memory descriptors or modify existing ones (e.g., for reserved kernel memory).

**high**
Address of last byte in memory region. The ten least significant address bits are all hardwired to 1.

**low**
Address of first byte in memory region. The ten least significant address bits are all hardwired to 0.

**v**
Indicates whether memory descriptor refers to physical memory (v = 0) or virtual memory (v = 1).

**type**
Identifies the type of the memory descriptor.

<table>
<thead>
<tr>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Undefined</td>
</tr>
<tr>
<td>0x1</td>
<td>Conventional memory</td>
</tr>
<tr>
<td>0x2</td>
<td>Reserved memory (i.e., reserved by kernel)</td>
</tr>
<tr>
<td>0x3</td>
<td>Dedicated memory (i.e., memory not available to user)</td>
</tr>
<tr>
<td>0x4</td>
<td>Shared memory (i.e., available to all users)</td>
</tr>
<tr>
<td>0xE</td>
<td>Defined by boot loader</td>
</tr>
<tr>
<td>0xF</td>
<td>Architecture dependent</td>
</tr>
</tbody>
</table>

**t**
Identifies the precise type for boot loader specific or architecture dependent memory descriptors.
The type of the memory descriptor is dependent on the bootloader. The $t$ field specifies the exact semantics. Refer to boot loader specification for more info.

The type of the memory descriptor is architecture dependent. The $t$ field specifies the exact semantics. Refer to architecture specific part for more info (see page 113).

The type of the memory descriptor is solely defined by the $type$ field. The content of the $t$ field is undefined.
Appendix A

IA-32 Interface
A.1 Virtual Registers [ia32]

Thread Control Registers (TCRs)

TCRs are implemented as part of the ia32-specific user-level thread control block (UTCB). The address of the current thread’s UTCB will not change over the lifetime of the thread. Setting the UTCB address of an active thread via THREADCONTROL is similar to deletion and re-creation. There is a fixed correlation between the UtcbLocation parameter when invoking THREADCONTROL and the UTCB address. The UTCB address of the current thread can be loaded through a machine instruction

\[
\text{mov} \quad \%\text{gs}[:0], \%r
\]

UTCB objects of the current thread can then be accessed as any other memory object. UTCBs of other threads must not be accessed, even if they are physically accessible. ThreadWord0 and ThreadWord1 are free to be used by systems software (e.g., IDL compilers). The kernel associates no semantics with these words.

\[
\begin{array}{|l|c|}
\hline
\sim (32) & \text{UTCB address} \\
\hline
\vdots & \vdots \\
\hline
\text{ThreadWord0} (32) & -16 \\
\hline
\text{ThreadWord1} (32) & -20 \\
\hline
\text{VirtualSender/ActualSender} (32) & -24 \\
\hline
\text{IntendedReceiver} (32) & -28 \\
\hline
\text{XferTimeouts} (32) & -32 \\
\hline
\text{ErrorCode} (32) & -36 \\
\hline
\sim (16) & \text{cop flags} (8) \\
\hline
\text{ExceptionHandler} (32) & -40 \\
\hline
\text{Pager} (32) & -44 \\
\hline
\text{UserDefinedHandle} (32) & -48 \\
\hline
\hline
\text{Preempt flags} (8) & \\
\hline
\end{array}
\]

MyLocalId = UTCB address (32)

\[
\begin{array}{|l|}
\hline
\text{gs}[:0] \\
\hline
\end{array}
\]

The TCR MyLocalId is not part of the UTCB. On ia32 it is identical with the UTCB address and can be loaded from memory location gs[:0].
**Message Registers (MRs)**

Memory-mapped MRs are implemented as part of the ia32-specific user-level thread control block (UTCB). The address of the current thread’s UTCB will not change over the lifetime of the thread. Setting the UTCB address of an active thread via THREADCONTROL is similar to deletion and re-creation. There is a fixed correlation between the UtcbLocation parameter when invoking THREADCONTROL and the UTCB address. The UTCB address of the current thread can be loaded through a machine instruction

\[
\text{mov } \%gs:[0], \%r
\]

UTCB objects of the current thread can then be accessed as any other memory object. UTCBs of other threads must not be accessed, even if they are physically accessible.

MR 0 is always mapped to a general register. MR 1 and MR 2 are mapped to general registers when reading a received message; in all other cases, MR 1 and MR 2 are mapped to memory locations. MR 3...63 are always mapped to memory.

\[
\begin{array}{|c|}
\hline
\text{MR 0} \\
\text{ESI} \\
\hline
\end{array}
\]

\[
\begin{array}{|c|}
\hline
\text{MR 1 (only for msg receive)} \\
\text{EBX} \\
\hline
\end{array}
\]

\[
\begin{array}{|c|}
\hline
\text{MR 2 (only for msg receive)} \\
\text{EBP} \\
\hline
\end{array}
\]

\[
\begin{array}{|c|}
\hline
\text{MR 1...63 [UTCB fields]} \\
\text{MR 63 (32)} & +252 \\
\vdots & \vdots \\
\text{MR 4 (32)} & +16 \\
\text{MR 3 (32)} & +12 \\
\text{MR 2 (except for msg receive) (32)} & +8 \\
\text{MR 1 (except for msg receive) (32)} & \text{UTCB address + 4} \\
\hline
\end{array}
\]

**Buffer Registers (BRs)**

BRs are implemented as part of the ia32-specific user-level thread control block (UTCB). The address of the current thread’s UTCB will not change over the lifetime of the thread. Setting the UTCB address of an active thread via THREADCONTROL is similar to deletion and re-creation. There is a fixed correlation between the UtcbLocation parameter when invoking THREADCONTROL and the UTCB address. The UTCB address of the current thread can be loaded through a machine instruction

\[
\text{mov } \%gs:[0], \%r
\]

UTCB objects of the current thread can then be accessed as any other memory object. UTCBs of other threads must not be accessed, even if they are physically accessible.
**VIRTUAL REGISTERS**

<table>
<thead>
<tr>
<th>BR 0...32 [UTCB fields]</th>
</tr>
</thead>
<tbody>
<tr>
<td>~ (32)</td>
</tr>
<tr>
<td>BR 0 (32)</td>
</tr>
<tr>
<td>BR 1 (32)</td>
</tr>
<tr>
<td>...</td>
</tr>
<tr>
<td>BR 32 (32)</td>
</tr>
</tbody>
</table>

**UTCB Memory With Undefined Semantics**

The kernel will associate no semantics with memory located at `UTCB address`...`UTCB address` + 3. The application can use this memory as thread local storage, e.g., for implementing the L4 API. Note, however, that the memory contents within this region may be overwritten during a system-call operating on message registers.

All undefined UTCB memory which is not covered by the above mentioned region may have kernel defined semantics.
A.2 Systemcalls

The system-calls which are invoked by the call instruction take the target of the calls the from system-call link fields in the kernel interface page (see page 2). Each system-call link specifies an address relative to the kernel interface page’s base address. An application may use instructions other than call to invoke the system-calls, but must ensure that a valid return address resides on the stack.

**KERNEL INTERFACE** [Slow Systemcall]

- EAX
- ECX
- EDX
- ESI
- EDI
- EBX
- EBP
- ESP

- KernelInterface →
  - EAX base address
  - ECX API Version
  - EDX API Flags
  - ESI Kernel ID
  - EDI ≡
  - EBX ≡
  - EBP ≡
  - ESP ≡

**EXCHANGE REGISTERS** [Systemcall]

- dest
- control
- SP
- IP
- EAX
- ECX
- EDX
- ESI
- EDI
- EBX
- EBP
- ESP

- Exchange Registers →
  - EAX result
  - ECX control
  - EDX SP
  - ESI IP
  - EDI FLAGS
  - EBX UserDefinedHandle
  - EBP pager
  - ESP ≡

“FLAGS” refers to the user-modifiable ia32 processor flags that are held in the EFLAGS register.

**THREAD CONTROL** [Privileged Systemcall]

- dest
- Pager
- Scheduler
- SpaceSpecifier
- UtcbLocation
- EAX
- ECX
- EDX
- ESI
- EDI
- EBX
- EBP
- ESP

- Thread Control →
  - EAX result
  - ECX ~
  - EDX ~
  - ESI ~
  - EDI ~
  - EBX ~
  - EBP ~
  - ESP ≡

**SYSTEM CLOCK** [Systemcall]

- EAX
- ECX
- EDX
- ESI
- EDI
- EBX
- EBP
- ESP

- SystemClock →
  - EAX clock 0...31
  - ECX ~
  - EDX clock 32...63
  - ESI ~
  - EDI ≡
  - EBX ≡
  - EBP ≡
  - ESP ≡
### THREADSWITCH [Systemcall]

<table>
<thead>
<tr>
<th>dest</th>
<th>EAX</th>
</tr>
</thead>
</table>
| − ECX | EAX  
| − EDX | ECX  
| − ESI | EDX  
| − EDI | ESI  
| − EBX | EDI  
| − EBP | EBX  
| − ESP | EBP  

*ThreadSwitch →*

<table>
<thead>
<tr>
<th>EAX</th>
</tr>
</thead>
</table>
| ECX  
| EDX  
| ESI  
| EDI  
| EBX  
| EBP  
| ESP  

*call ThreadSwitch*

### SCHEDULE [Systemcall]

<table>
<thead>
<tr>
<th>dest</th>
<th>EAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>prio</td>
<td>ECX</td>
</tr>
<tr>
<td>time control</td>
<td>EDX</td>
</tr>
<tr>
<td>processor control</td>
<td>ESI</td>
</tr>
<tr>
<td>preemption control</td>
<td>EDI</td>
</tr>
</tbody>
</table>
| − EBX | EDX  
| − EBP | ESI  
| − ESP | EDI  

*SCHEDULE →*

<table>
<thead>
<tr>
<th>EAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>result</td>
</tr>
<tr>
<td>− time control</td>
</tr>
<tr>
<td>− processor control</td>
</tr>
<tr>
<td>− preemption control</td>
</tr>
</tbody>
</table>
| − EBX | EDX  
| − EBP | ESI  
| − ESP | EDI  

*call Schedule*

### IPC [Systemcall]

<table>
<thead>
<tr>
<th>to</th>
<th>EAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timeouts</td>
<td>ECX</td>
</tr>
<tr>
<td>FromSpecifier</td>
<td>EDX</td>
</tr>
<tr>
<td>MR0</td>
<td>ESI</td>
</tr>
<tr>
<td>UTCP</td>
<td>EDI</td>
</tr>
</tbody>
</table>
| − EBX | EDX  
| − EBP | ESI  
| − ESP | EDI  

*IPC →*

<table>
<thead>
<tr>
<th>EAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>from</td>
</tr>
<tr>
<td>− Timeouts</td>
</tr>
<tr>
<td>− FromSpecifier</td>
</tr>
<tr>
<td>− MR0</td>
</tr>
</tbody>
</table>
| − EBX | EDX  
| − EBP | ESI  
| − ESP | EDI  

*call Ipc*

### LIPC [Systemcall]

<table>
<thead>
<tr>
<th>to</th>
<th>EAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timeouts</td>
<td>ECX</td>
</tr>
<tr>
<td>FromSpecifier</td>
<td>EDX</td>
</tr>
<tr>
<td>MR0</td>
<td>ESI</td>
</tr>
<tr>
<td>UTCP</td>
<td>EDI</td>
</tr>
</tbody>
</table>
| − EBX | EDX  
| − EBP | ESI  
| − ESP | EDI  

*LIPC →*

<table>
<thead>
<tr>
<th>EAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>from</td>
</tr>
<tr>
<td>− Timeouts</td>
</tr>
<tr>
<td>− FromSpecifier</td>
</tr>
<tr>
<td>− MR0</td>
</tr>
</tbody>
</table>
| − EBX | EDX  
| − EBP | ESI  
| − ESP | EDI  

*call Lipc*

### UNMAP [Systemcall]

<table>
<thead>
<tr>
<th>control</th>
<th>EAX</th>
</tr>
</thead>
</table>
| − ECX | EAX  
| − EDX | ECX  
| MR0 | EDX  
| UTCP | ESI  
| − EBX | EDX  
| − EBP | ESI  
| − ESP | ESI  

*UNMAP →*

<table>
<thead>
<tr>
<th>control</th>
<th>EAX</th>
</tr>
</thead>
</table>
| − ECX | ECX  
| − EDX | EDX  
| MR0 | ESI  
| UTCP | EDI  
| − EBX | EDX  
| − EBP | ESI  
| − ESP | ESI  

*call Unmap*
### SPACECONTROL

**[Privileged Systemcall]**

<table>
<thead>
<tr>
<th>SpaceSpecifier control</th>
<th>EAX</th>
<th>→</th>
<th>EAX control result</th>
</tr>
</thead>
<tbody>
<tr>
<td>KernelInterfacePageArea</td>
<td>ECX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>UtechArea Redirector</td>
<td>EDX</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ESI</td>
<td>∼</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EDI</td>
<td>EAX</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EBX</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>EBP</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ESP</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**call SpaceControl**

### PROCESSORCONTROL

**[Privileged Systemcall]**

<table>
<thead>
<tr>
<th>ProcessorNo</th>
<th>EAX</th>
<th>→</th>
<th>EAX control result</th>
</tr>
</thead>
<tbody>
<tr>
<td>InternalFrequency</td>
<td>ECX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ExternalFrequency</td>
<td>EDX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>voltage</td>
<td>ESI</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>EDI</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>EBX</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>EBP</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ESP</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**call ProcessorControl**

### MEMORYCONTROL

**[Privileged Systemcall]**

<table>
<thead>
<tr>
<th>control</th>
<th>EAX</th>
<th>→</th>
<th>EAX control result</th>
</tr>
</thead>
<tbody>
<tr>
<td>attribute0</td>
<td>ECX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>attribute1</td>
<td>EDX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MR0</td>
<td>ESI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>UTCB</td>
<td>EDI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>attribute2</td>
<td>EBX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>attribute3</td>
<td>EBP</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ESP</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**call MemoryControl**
A.3 Kernel Features [ia32]

The ia32 architecture supports the following kernel feature descriptors in the kernel interface page (see page 5).

<table>
<thead>
<tr>
<th>String</th>
<th>Feature</th>
</tr>
</thead>
<tbody>
<tr>
<td>“smallspaces”</td>
<td>Kernel has small address spaces enabled.</td>
</tr>
</tbody>
</table>
A.4 IO-Ports [ia32]

On ia32 processors, IO-ports are handled as fpages. IO fpages can be mapped, granted, and unmapped like memory fpages. Their minimal granularity is 1. An IO-fpage of size $2^s$ has a $2^s$-aligned base address $p$, i.e. $p \mod 2^s = 0$. An fpage with base port address $p$ and size $2^s$ is denoted as described below.

$$IO \text{fpage} \ (p, 2^s)$$

| $p$ (16/48) | $s$ (6) | $s = 2^s$ (6) | 0 r w x |

IO-ports can only be mapped idempotently, i.e., physical port $x$ is either mapped at IO address $x$ in the task’s IO address space, or it is not mapped at all.

---

**Generic Programming Interface**

```
#include <l4/space.h>

Fpage IoFpage (Word BaseAddress, int FpageSize)
Fpage IoFpageLog2 (Word BaseAddress, int Log2FpageSize < 64)
```

Delivers an IO fpage with the specified location and size.
### A.5 Space Control  [ia32]

The SPACECONTROL system call has an architecture dependent control parameter to specify various address space characteristics. For ia32, the control parameter has the following semantics.

#### Input Parameter

<table>
<thead>
<tr>
<th>control</th>
</tr>
</thead>
<tbody>
<tr>
<td>s</td>
</tr>
<tr>
<td>0 (23)</td>
</tr>
<tr>
<td>small (8)</td>
</tr>
</tbody>
</table>

- **s**: A value of 1 indicates the intention to change the *small address space number* for the specified address space. The small space number will remain unchanged if \( s = 0 \).

- **small**: If \( s = 1 \), sets the small address space number for the specified address space. Small address space numbers from 1 to 255 are available. A value of 0 indicates a regular large address space. An assigned small space number is effective on all CPUs in an SMP system.

The position \( pos \) of the least significant bit of small indicates the size of the small space by the following formula: \( size = 2^{pos} \times 4 \) MB. After removing the least significant bit, the remaining bits of small indicate the location of the space within a 512 MB region using the following formula: \( location = small \times 2 \) MB. Setting the small space number fails if the specified region overlaps with an already existing one.

The small field is ignored if \( s = 0 \), or if the kernel does not support small spaces (see Kernel Features, page 92).

#### Output Parameter

<table>
<thead>
<tr>
<th>control</th>
</tr>
</thead>
<tbody>
<tr>
<td>e</td>
</tr>
<tr>
<td>0 (23)</td>
</tr>
<tr>
<td>small (8)</td>
</tr>
</tbody>
</table>

- **e**: Indicates if the change of small space number was effective \( (e = 1) \). Undefined if \( s = 0 \) in the input parameter.

- **small**: The old value for the small space number. A value of 0 is possible even if the space has previously been put into a small address space. An implicit change to small space number 0 can happen if a thread within the space accesses memory beyond the specified small space size.

#### Generic Programming Interface

```c
#include <l4/space.h>

Word LargeSpace

Word SmallSpace (Word location, size)

Delivers a small space number with the specified location and size (both in MB). It is assumed that \( size = 2^p \times 4 \) for some value \( p < 8 \).```
A.6 Cacheability Hints  [ia32]

String items can specify cacheability hints to the kernel (see page 52). For ia32, the cacheability hints have the following semantics.

\[ hh = 00 \] Use the processor’s default cacheability strategy. Typically, cache lines are allocated for data read and written (assuming that the processor’s default strategy is write-back and write-allocate).

\[ hh = 01 \] Allocate cache lines in the entire cache hierarchy for data read or written.

\[ hh = 10 \] Do not allocate new cache lines (entire cache hierarchy) for data read or written.

\[ hh = 11 \] Allocate only new L1 cache line for data read or written. Do not allocate cache lines in lower cache hierarchies.

Convenience Programming Interface

```
#include <l4/ipc.h>

CacheAllocationHint UseDefaultCacheLineAllocation
CacheAllocationHint AllocateNewCacheLines
CacheAllocationHint DoNotAllocateNewCacheLines
CacheAllocationHint AllocateOnlyNewL1CacheLines
```
A.7 Memory Attributes  [ia32]

The ia32 architecture in general supports the following memory attributes values.

<table>
<thead>
<tr>
<th>attribute</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Default</td>
<td>0</td>
</tr>
<tr>
<td>Uncacheable</td>
<td>1</td>
</tr>
<tr>
<td>Write Combining</td>
<td>2</td>
</tr>
<tr>
<td>Write Through</td>
<td>5</td>
</tr>
<tr>
<td>Write Protected</td>
<td>6</td>
</tr>
<tr>
<td>Write Back</td>
<td>7</td>
</tr>
</tbody>
</table>

Note that some attributes are only supported on certain processors. See the “IA-32 Intel Architecture Software Developer’s Manual, Volume 3: System Programming Guide” for the semantics of the memory attributes and which processors they are supported on.

---

Generic Programming Interface

```c
#include <l4/misc.h>

Word DefaultMemory
Word UncacheableMemory
Word WriteCombiningMemory
Word WriteThroughMemory
Word WriteProtectedMemory
Word WriteBackMemory
```
A.8 Exception Message Format

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>EAX (32)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ECX (32)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EDX (32)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EBX (32)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESP (32)</td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EBP (32)</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESI (32)</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EDI (32)</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ErrorCode (32)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ExceptionNo (32)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EFLAGS (32)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EIP (32)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note that executing an INT \( n \) instructions in 32-bit mode will always raise a #GP (general protection). The exception handler may interpret the error code \((8n + 2\) see processor manual) and emulate the INT \( n \) accordingly.

#PF (page fault), #MC (machine check exception), and some #GP (general protection), #SS (stack segment fault), and #NM (no math coprocessor) exceptions are handled by the kernel and therefore do not generate exception messages.
A.9 Processor Mirroring

**Segments**

L4 uses a flat (unsegmented) memory model. There are only three segments available: `user_space`, a read/write segment, `user_space_exec`, an executable segment, and `utcb_address`, a read-only segment. Both `user_space` and `user_space_exec` cover (at least) the complete user-level address space. `Utcb_address` covers only enough memory to hold the UTCB address.

The values of segment selectors are undefined. When a thread is created, its segment registers SS, DS, ES and FS are initialized with `user_space`, GS with `utcb_address`, and CS with `user_space_exec`. Whenever the kernel detects a general protection exception and the segment registers are not loaded properly, it reloads them with the above mentioned selectors. From the user’s point of view, the segment registers cannot be modified.

However, the binary representation of `user_space` and `user_space_exec` may change at any point during program execution. Never rely on any particular value.

Furthermore, the LSL (load segment limit) machine instruction may deliver wrong segment limits, even floating ones. The result of this instruction is always undefined.

**Debug Registers**

User-level debug registers exist per thread. DR0…3, DR6 and DR7 can be accessed by the machine instructions `mov n,DRx` and `mov DRx,r`. However, only task-local breakpoints can be activated, i.e., bits G0…3 in DR7 cannot be set. Breakpoints operate per thread. Breakpoints are signaled as #DB exception (INT 1).

Note that user-level breakpoints are suspended when kernel breakpoints are set by the kernel debugger.

**Model-Specific Registers**

All privileged threads in the system have read and write access to all the Model-Specific Registers (MSRs) of the CPU. Modification of some MSRs may lead to undefined system behavior. Any access to an MSR by an unprivileged thread will raise an exception.
A.10 Booting

PC-compatible Machines

L4 can be loaded at any 16-byte-aligned location beyond 0x1000 in physical memory. It can be started in real mode or in 32-bit protected mode at address 0x100 or 0x1000 relative to its load address. The protected-mode conditions are compliant to the Multiboot Standard Version 0.6.

<table>
<thead>
<tr>
<th>Start Preconditions</th>
<th>Real Mode</th>
<th>32-bit Protected Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>load base ((L))</td>
<td>(L \geq 0x1000, 16)-byte aligned</td>
<td>(L \geq 0x1000)</td>
</tr>
<tr>
<td>load offset ((X))</td>
<td>(X = 0x100) or (X = 0x1000)</td>
<td>(X = 0x100) or (X = 0x1000)</td>
</tr>
<tr>
<td>Interrupts</td>
<td>disabled</td>
<td>disabled</td>
</tr>
<tr>
<td>Gate A20</td>
<td>~</td>
<td>open</td>
</tr>
<tr>
<td>EFLAGS</td>
<td>I=0</td>
<td>I=0, VM=0</td>
</tr>
<tr>
<td>CR0</td>
<td>PE=0</td>
<td>PE=1, PG=0</td>
</tr>
<tr>
<td>(E)IP</td>
<td>(X)</td>
<td>(L + X)</td>
</tr>
<tr>
<td>CS</td>
<td>(L/16)</td>
<td>0, 4GB, 32-bit exec</td>
</tr>
<tr>
<td>SS, DS, ES</td>
<td>~</td>
<td>0, 4GB, read/write</td>
</tr>
<tr>
<td>EAX</td>
<td>~</td>
<td>0x2BADB002</td>
</tr>
<tr>
<td>EBX</td>
<td>~</td>
<td>~P</td>
</tr>
<tr>
<td>((P + 0))</td>
<td>n/a</td>
<td>~ OR 1</td>
</tr>
<tr>
<td>((P + 4))</td>
<td></td>
<td>below 640 K mem in K</td>
</tr>
<tr>
<td>((P + 8))</td>
<td></td>
<td>beyond 1M mem in K</td>
</tr>
<tr>
<td>all remaining registers &amp; flags</td>
<td>~</td>
<td>~</td>
</tr>
</tbody>
</table>

L4 relocates itself to 0x1000, enters protected mode if started in real mode, enables paging and initializes itself.
B.1 Virtual Registers

Thread Control Registers (TCRs)

TCRs are mapped to memory locations. They are implemented as part of the ia64-specific user-level thread control block (UTCB). The address of the current thread’s UTCB will not change over the lifetime of the thread. (In fact, the ia64 UTCB address is identical to the thread’s local ID.) Register ar.k6 always contains the UTCB address of the current thread. UTCBs of other threads must not be accessed, even if they are physically accessible. ThreadWord0 and ThreadWord1 are free to be used by systems software (e.g., IDL compilers). The kernel associates no semantics with these words.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Offset from UTCB Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>ThreadWord 1 (64)</td>
<td>+352</td>
</tr>
<tr>
<td>ThreadWord 0 (64)</td>
<td>+344</td>
</tr>
<tr>
<td>ErrorCode (64)</td>
<td>+72</td>
</tr>
<tr>
<td>VirtualSender/ActualSender (64)</td>
<td>+64</td>
</tr>
<tr>
<td>IntendedReceiver (64)</td>
<td>+56</td>
</tr>
<tr>
<td>XferTimeouts (64)</td>
<td>+48</td>
</tr>
<tr>
<td>~ (48)</td>
<td></td>
</tr>
<tr>
<td>cop flags (8)</td>
<td></td>
</tr>
<tr>
<td>preempt flags (8)</td>
<td></td>
</tr>
<tr>
<td>ExceptionHandler (64)</td>
<td>+32</td>
</tr>
<tr>
<td>Pager (64)</td>
<td>+24</td>
</tr>
<tr>
<td>UserDefinedHandle (64)</td>
<td>+16</td>
</tr>
<tr>
<td>ProcessorNo (64)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>← UTCB address + 8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>MyLocalId = UTCB address (64)</td>
<td>ar.k6</td>
</tr>
<tr>
<td>MyGlobalId (64)</td>
<td>ar.k5</td>
</tr>
</tbody>
</table>

Message Registers (MRs)

Memory-mapped MRs are implemented as part of the ia64-specific user-level thread control block (UTCB). The address of the current thread’s UTCB will not change over the lifetime of the thread. (In fact, the ia64 UTCB address is identical to the thread’s local ID.) Register ar.k6 always contains the UTCB address of the current thread. UTCBs of other threads must not be accessed, even if they are physically accessible.

MR[0, 7] are mapped to the eight first output registers on the register stack. The exact location of the first eight message registers therefore depends on the configuration of the current frame marker (CFM). MR[8, 63] are mapped to memory. It is valid to configure less than eight output registers in the current register frame if a message to be transferred spans less than eight message registers. The number of message registers must not exceed the number of output registers, however.
**VIRTUAL REGISTERS**

### Buffer Registers (BRs)

BRs are implemented as part of the ia64-specific user-level thread control block (UTCB). The address of the current thread’s UTCB will not change over the lifetime of the thread. (In fact, the ia64 UTCB address is identical to the thread’s local ID.) Register ar.k6 always contains the UTCB address of the current thread. UTCBs of other threads must not be accessed, even if they are physically accessible.

### UTCB Memory With Undefined Semantics

The kernel will associate no semantics with memory located at \( UTCB\ address + 384 \ldots UTCB\ address + 447 \). The application can use this memory as thread local storage, e.g., for implementing the L4 API. Note, however, that the memory contents within this region may be overwritten during a system-call operating on message registers.

All undefined UTCB memory which is not covered by the above mentioned region may have kernel defined semantics.
The microkernel provides special system-calls for accessing Processor Abstraction Level (PAL) and System Abstraction Layer (SAL) procedures. The location of the additional system-call links in the kernel interface page are as follows:

<table>
<thead>
<tr>
<th>Location</th>
<th>System-call</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kernel Interface Page + 0x220</td>
<td>PAL_CALL</td>
</tr>
<tr>
<td>Kernel Interface Page + 0x228</td>
<td>SAL_CALL</td>
</tr>
</tbody>
</table>

**Generic Programming Interface**

**System-Call Function:**

```c
#include <l4/arch.h>

Word PAL_Call (Word idx, a1, a2, a3, Word& r1, r2, r3)
Invoke the PAL procedure specified by idx. a1...a3 are the arguments to the PAL procedure. r1...r3 are the return values. The system-call returns the status of the procedure invocation. See the “Intel Itanium Architecture Software Developer’s Manual, Volume 2: System Architecture” for the possible values of idx, and the contents of arguments and return values.
As of now, no invocation of PAL procedures is allowed by any user-level thread.
```

```c
Word SAL_Call (Word idx, a1, a2, a3, a4, a5, a6, Word& r1, r2, r3)
Invoke the SAL procedure specified by idx. a1...a6 are the arguments to the SAL procedure. r1...r3 are the return values. The system-call returns the status of the procedure invocation. See the “Itanium Processor Family System Abstraction Layer Specification” for possible values of idx, and the contents of arguments and return values.
As of now, only the PCI_CONFIG_READ and PCI_CONFIG_WRITE procedure calls can be invoked from a user-level thread.
```

**Convenience Programming Interface**

**Derived Functions:**

```c
#include <l4/arch.h>

Word SAL_PCI_ConfigRead (Word address, size, Word& value)
Read from the PCI configuration space at address with the indicated word size (1, 2 or 4 bytes). The read value is returned in value. Return the status of the operation (0 if success). The operation will only succeed if the address in the PCI configuration space is mapped readable (see page 110)
```

```c
Word SAL_PCI_ConfigWrite (Word address, size, value)
Write value to the PCI configuration space at address with the indicated word size (1, 2 or 4 bytes). Return the status of the operation (0 if success). The operation will only succeed if the address in the PCI configuration space is mapped writeable (see page 110).
```
B.3 Systemcalls [ia64]

The system-calls which are invoked by the br.call instruction take the target of the calls from system-call link fields in the kernel interface page (see page 2). Each system-call link value, \( v \), specifies either an absolute address (if \( v \geq 1\text{MB} \)) or an address relative to the kernel interface page’s base address (if \( v < 1\text{MB} \)). An application may use instructions other than br.call to invoke the system-calls, but must ensure that a valid return address resides in the b0 register for the IPC and LIPC system-calls the application must additionally ensure that message registers are mapped into input registers after invoking the system-call (i.e., the output registers if one were to use a br.call instruction).

The system-call definitions below only specify the contents of the general registers. Except for the KERNELINTERFACE, IPC and LIPC system-calls, the contents of the remaining user accessible registers closely resembles the IA-64 software calling conventions. More precisely, the register contents of these registers are ignored upon system-call entry, and the contents after system-call exit are defined as follows:

**Floating-point Registers:**
- \( f0 \ldots f1 \) fixed
- \( f2 \ldots f5 \) preserved
- \( f6 \ldots f15 \) scratch
- \( f16 \ldots f27 \) preserved

**Predicate Registers:**
- \( p0 \) fixed
- \( p1 \ldots p5 \) preserved
- \( p6 \ldots p15 \) scratch
- \( p16 \ldots p27 \) preserved

**Branch Registers:**
- \( b0 \) system-call return address
- \( b1 \ldots b5 \) preserved
- \( b6 \ldots b7 \) scratch

**Application Registers:**
- \( ar.fpsr \) special (see below)
- \( ar.rnat \) preserved
- \( ar.unat \) preserved
- \( ar.ps \) scratch
- \( ar.bsp \) preserved
- \( ar.bpstore \) preserved
- \( ar.rsc \) special (see below)
- \( ar.ie \) preserved
- \( ar.ec \) preserved
- \( ar.cc \) scratch
- \( ar.itc \) scratch
- \( ar.k1 \ldots k4 \) scratch
- \( ar.k5 \) MyGlobalId
- \( ar.k6 \) MyLocalId
- \( ar.k7 \) scratch

The \( ar.fpsr \) and \( ar.rsc \) registers are special. The second and third status fields of \( ar.fpsr \) and the loadrs field of \( ar.rsc \) have scratch semantics. The remaining fields have preserved semantics.

---

**KERNELINTERFACE** [Slow Systemcall]

\[
\begin{array}{c|c}
\text{KernelInterface} & \text{KernelInterface} \\
\hline
r1 \ldots r7 & r1 \ldots r7 \\
r8 & r8 \\
r9 & r9 \\
r10 & r10 \\
r11 & r11 \\
r12 \ldots r31 & r12 \ldots r31 \\
u0 \ldots u95 & u0 \ldots u95 \\
loc0 \ldots loc95 & loc0 \ldots loc95 \\
\text{out0} \ldots \text{out95} & \text{out0} \ldots \text{out95} \\
\end{array}
\]

All other registers remain unchanged. A qualifying predicate, \( qp \), can be used to conditionally execute the KERNELINTERFACE system-call.
### EXCHANGE_REGISTERS  
**[Systemcall]**  

```
<table>
<thead>
<tr>
<th>dest</th>
<th>r1</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>r2...r3</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>r4...r7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>r8...r11</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>r12...r13</td>
<td></td>
</tr>
<tr>
<td></td>
<td>r14</td>
<td></td>
</tr>
<tr>
<td></td>
<td>r15</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SP</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IP</td>
<td></td>
</tr>
<tr>
<td></td>
<td>FLAGS</td>
<td></td>
</tr>
<tr>
<td></td>
<td>UserDefinedHandle</td>
<td></td>
</tr>
<tr>
<td></td>
<td>pager</td>
<td></td>
</tr>
<tr>
<td></td>
<td>r21...r31</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>out0...out95</td>
<td>~</td>
</tr>
</tbody>
</table>
```

- `br.call b0 = ExchangeRegisters`

### THREAD_CONTROL  
**[Privileged Systemcall]**

```
<table>
<thead>
<tr>
<th>dest</th>
<th>r1</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>r2...r3</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>r4...r7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>r8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>r9...r11</td>
<td></td>
</tr>
<tr>
<td></td>
<td>r12...r13</td>
<td></td>
</tr>
<tr>
<td></td>
<td>r14</td>
<td></td>
</tr>
<tr>
<td></td>
<td>r15</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SpaceSpecifier</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Scheduler</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pager</td>
<td></td>
</tr>
<tr>
<td></td>
<td>UtcbLocation</td>
<td></td>
</tr>
<tr>
<td></td>
<td>r19...r31</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>out0...out95</td>
<td>~</td>
</tr>
</tbody>
</table>
```

- `br.call b0 = ThreadControl`

### SYSTEM_CLOCK  
**[Systemcall]**

```
<table>
<thead>
<tr>
<th>dest</th>
<th>r1</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>r2...r3</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>r4...r7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>r8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>r9...r11</td>
<td></td>
</tr>
<tr>
<td></td>
<td>r12...r13</td>
<td></td>
</tr>
<tr>
<td></td>
<td>r14...r31</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>out0...out95</td>
<td>~</td>
</tr>
</tbody>
</table>
```

- `br.call b0 = SystemClock`

### THREAD_SWITCH  
**[Systemcall]**

```
<table>
<thead>
<tr>
<th>dest</th>
<th>r1</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>r2...r3</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>r4...r7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>r8...r11</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>r12...r13</td>
<td></td>
</tr>
<tr>
<td></td>
<td>r14</td>
<td></td>
</tr>
<tr>
<td></td>
<td>r15...r31</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>out0...out95</td>
<td>~</td>
</tr>
</tbody>
</table>
```

- `br.call b0 = ThreadSwitch`
### SCHEDULE [Systemcall]

<table>
<thead>
<tr>
<th>Schedule</th>
<th>b0 = Schedule</th>
</tr>
</thead>
<tbody>
<tr>
<td>r1</td>
<td>r1</td>
</tr>
<tr>
<td>r2...r3</td>
<td>r2...r3</td>
</tr>
<tr>
<td>r4...r7</td>
<td>r4...r7</td>
</tr>
<tr>
<td>r8</td>
<td>result</td>
</tr>
<tr>
<td>r9</td>
<td>time control</td>
</tr>
<tr>
<td>r10...r11</td>
<td>r10...r11</td>
</tr>
<tr>
<td>r12...r13</td>
<td>r12...r13</td>
</tr>
<tr>
<td>r14</td>
<td>r14</td>
</tr>
<tr>
<td>r15</td>
<td>r15</td>
</tr>
<tr>
<td>r16</td>
<td>r16</td>
</tr>
<tr>
<td>r17</td>
<td>r17</td>
</tr>
<tr>
<td>r18</td>
<td>r18</td>
</tr>
<tr>
<td>r19...r31</td>
<td>r19...r31</td>
</tr>
<tr>
<td>dest</td>
<td>result</td>
</tr>
<tr>
<td>time control</td>
<td>time control</td>
</tr>
<tr>
<td>processor control</td>
<td>processor control</td>
</tr>
<tr>
<td>prio</td>
<td>result</td>
</tr>
<tr>
<td>preemption control</td>
<td>result</td>
</tr>
</tbody>
</table>

All remaining registers (including application registers) will have scratch semantics over the SCHEDULE system-call. Upon entry to the SCHEDULE system-call, the register stack backing store must be able to contain the dirty partition of the register stack.

### IPC [Systemcall]

<table>
<thead>
<tr>
<th>Ipc</th>
<th>b0 = Ipc</th>
</tr>
</thead>
<tbody>
<tr>
<td>r1</td>
<td>r1</td>
</tr>
<tr>
<td>r2...r8</td>
<td>r2...r8</td>
</tr>
<tr>
<td>r9</td>
<td>from</td>
</tr>
<tr>
<td>r10...r11</td>
<td>r10...r11</td>
</tr>
<tr>
<td>r12</td>
<td>r12</td>
</tr>
<tr>
<td>r13</td>
<td>r13</td>
</tr>
<tr>
<td>r14</td>
<td>r14</td>
</tr>
<tr>
<td>r15</td>
<td>r15</td>
</tr>
<tr>
<td>r16</td>
<td>r16</td>
</tr>
<tr>
<td>r17...r31</td>
<td>r17...r31</td>
</tr>
<tr>
<td>MR0</td>
<td>out0</td>
</tr>
<tr>
<td>MR1</td>
<td>out1</td>
</tr>
<tr>
<td>MR2</td>
<td>out2</td>
</tr>
<tr>
<td>MR3</td>
<td>out3</td>
</tr>
<tr>
<td>MR4</td>
<td>out4</td>
</tr>
<tr>
<td>MR5</td>
<td>out5</td>
</tr>
<tr>
<td>MR6</td>
<td>out6</td>
</tr>
<tr>
<td>MR7</td>
<td>out7</td>
</tr>
<tr>
<td>out8...out95</td>
<td>out8...out95</td>
</tr>
</tbody>
</table>

All remaining registers (including application registers) will have scratch semantics over the IPC system-call. Upon entry to the IPC system-call, the register stack backing store must be able to contain the dirty partition of the register stack.

### LIPC [Systemcall]

<table>
<thead>
<tr>
<th>Lipc</th>
<th>b0 = Lipc</th>
</tr>
</thead>
<tbody>
<tr>
<td>r1</td>
<td>r1</td>
</tr>
<tr>
<td>r2...r8</td>
<td>r2...r8</td>
</tr>
<tr>
<td>r9</td>
<td>from</td>
</tr>
<tr>
<td>r10...r11</td>
<td>r10...r11</td>
</tr>
<tr>
<td>r12</td>
<td>r12</td>
</tr>
<tr>
<td>r13</td>
<td>r13</td>
</tr>
<tr>
<td>r14</td>
<td>r14</td>
</tr>
<tr>
<td>r15</td>
<td>r15</td>
</tr>
<tr>
<td>r16</td>
<td>r16</td>
</tr>
<tr>
<td>r17...r31</td>
<td>r17...r31</td>
</tr>
<tr>
<td>MR0</td>
<td>out0</td>
</tr>
<tr>
<td>MR1</td>
<td>out1</td>
</tr>
<tr>
<td>MR2</td>
<td>out2</td>
</tr>
<tr>
<td>MR3</td>
<td>out3</td>
</tr>
<tr>
<td>MR4</td>
<td>out4</td>
</tr>
<tr>
<td>MR5</td>
<td>out5</td>
</tr>
<tr>
<td>MR6</td>
<td>out6</td>
</tr>
<tr>
<td>MR7</td>
<td>out7</td>
</tr>
<tr>
<td>out8...out95</td>
<td>out8...out95</td>
</tr>
</tbody>
</table>
All remaining registers (including application registers) will have scratch semantics over the LPC system-call. Upon entry to the LPC system-call, the register stack backing store must be able to contain the dirty partition of the register stack.

**UNMAP**  [Systemcall]

\[
\begin{array}{c|c|c}
- & - & - \\
- & r1 & \equiv \\
- & r2 \ldots r3 & \sim \\
- & r4 \ldots r7 & \equiv \\
- & r8 \ldots r11 & \sim \\
- & r12 \ldots r13 & \equiv \\
\text{control} & r14 & \\
- & r16 \ldots r31 & \sim \\
\text{MR}_0 & \text{out0} & \\
\text{MR}_1 & \text{out1} & \\
\text{MR}_2 & \text{out2} & \\
\text{MR}_3 & \text{out3} & \\
\text{MR}_4 & \text{out4} & \\
\text{MR}_5 & \text{out5} & \\
\text{MR}_6 & \text{out6} & \\
\text{MR}_7 & \text{out7} & \\
- & \text{out8} \ldots \text{out95} & \\
\end{array}
\]

**SPACECONTROL**  [Privileged Systemcall]

\[
\begin{array}{c|c|c}
- & - & - \\
- & r1 & \equiv \\
- & r2 \ldots r3 & \sim \\
- & r4 \ldots r7 & \equiv \\
- & r8 & \sim \\
- & r9 & \\
- & \text{r10} \ldots \text{r11} & \equiv \\
- & \text{r12} \ldots \text{r13} & \sim \\
\text{specifier} & \text{control} & \text{r15} \\
\text{KernelInterfacePageArea} & \text{r16} & \\
\text{UtebArea} & \text{r17} & \\
\text{Redirector} & \text{r18} & \\
- & \text{r19} \ldots \text{r31} & \sim \\
- & \text{out0} \ldots \text{out95} & \\
\end{array}
\]

**PROCESSORCONTROL**  [Privileged Systemcall]

\[
\begin{array}{c|c|c}
- & - & - \\
- & r1 & \equiv \\
- & r2 \ldots r3 & \sim \\
- & r4 \ldots r7 & \equiv \\
- & r8 & \equiv \\
- & r9 \ldots r11 & \sim \\
- & \text{r12} \ldots \text{r13} & \equiv \\
\text{ProcessorNo} & \text{r14} & \\
\text{InternalFrequency} & \text{r15} & \\
\text{ExternalFrequency} & \text{r16} & \\
\text{voltage} & \text{r17} & \\
- & \text{r18} \ldots \text{r31} & \\
- & \text{out0} \ldots \text{out95} & \\
\end{array}
\]

\[
\begin{array}{c|c|c}
- & - & - \\
- & r1 & \equiv \\
- & r2 \ldots r3 & \sim \\
- & r4 \ldots r7 & \equiv \\
- & r8 & \sim \\
- & r9 \ldots r11 & \equiv \\
- & r12 \ldots r13 & \sim \\
\text{result} & \text{control} & \text{r15} \\
\text{out0} \ldots \text{out95} & \sim \\
\end{array}
\]

\[
\begin{array}{c|c|c}
- & - & - \\
- & r1 & \equiv \\
- & r2 \ldots r3 & \sim \\
- & r4 \ldots r7 & \equiv \\
- & r8 & \equiv \\
- & r9 \ldots r11 & \sim \\
- & r12 \ldots r13 & \equiv \\
\text{result} & \text{control} & \text{r15} \\
\text{out0} \ldots \text{out95} & \sim \\
\end{array}
\]

\[
\begin{array}{c|c|c}
- & - & - \\
- & r1 & \equiv \\
- & r2 \ldots r3 & \sim \\
- & r4 \ldots r7 & \equiv \\
- & r8 & \equiv \\
- & r9 \ldots r11 & \sim \\
- & r12 \ldots r13 & \equiv \\
\text{result} & \text{control} & \text{r15} \\
\text{out0} \ldots \text{out95} & \sim \\
\end{array}
\]

\[
\begin{array}{c|c|c}
- & - & - \\
- & r1 & \equiv \\
- & r2 \ldots r3 & \sim \\
- & r4 \ldots r7 & \equiv \\
- & r8 & \equiv \\
- & r9 \ldots r11 & \sim \\
- & r12 \ldots r13 & \equiv \\
\text{result} & \text{control} & \text{r15} \\
\text{out0} \ldots \text{out95} & \sim \\
\end{array}
\]
**MEMORY CONTROL**  
*Privileged Systemcall*

- `r1`  
- `r2`..`r3`  
- `r4`..`r7`  
- `r8`..`r11`  
- `r12`..`r13`  

**Control**  
- `control`  
- `attribute_0`  
- `attribute_1`  
- `attribute_2`  
- `attribute_3`  
- `MR_0`  
- `MR_1`  
- `MR_2`  
- `MR_3`  
- `MR_4`  
- `MR_5`  
- `MR_6`  
- `MR_7`  
- `MR_8`..`MR_95`  

**Memory Control**  
`br.call b0 = MemoryControl`

- `r1`  
- `r2`..`r3`  
- `r4`..`r7`  
- `r8`..`r11`  
- `r12`..`r13`  
- `r14`  
- `r15`  
- `r16`  
- `r17`  
- `r18`  
- `r19`..`r31`  

**PAL CALL**  
*Architecture Specific Systemcall*

- `r1`  
- `r2`..`r3`  
- `r4`..`r7`  
- `r8`  
- `r9`  
- `r10`  
- `r11`  
- `r12`..`r13`  
- `r14`..`r27`  
- `idx`  
- `arg_1`  
- `arg_2`  
- `arg_3`  
- `arg_4`..`arg_95`  

**PAL Call**  
`br.call b0 = PAL_Call`

- `r1`  
- `r2`..`r3`  
- `r4`..`r7`  
- `r8`  
- `r9`  
- `r10`  
- `r11`  
- `r12`..`r13`  
- `r14`..`r27`  
- `idx`  
- `arg_1`  
- `arg_2`  
- `arg_3`  
- `arg_4`..`arg_95`  

**SAL CALL**  
*Architecture Specific Systemcall*

- `r1`  
- `r2`..`r3`  
- `r4`..`r7`  
- `r8`  
- `r9`  
- `r10`  
- `r11`  
- `r12`..`r13`  
- `r14`..`r31`  
- `idx`  
- `arg_1`  
- `arg_2`  
- `arg_3`  
- `arg_4`  
- `arg_5`  
- `arg_6`  
- `arg_7`..`arg_95`  

**SAL Call**  
`br.call b0 = SAL_Call`

- `r1`  
- `r2`..`r3`  
- `r4`..`r7`  
- `r8`  
- `r9`  
- `r10`  
- `r11`  
- `r12`..`r13`  
- `r14`..`r31`  
- `idx`  
- `arg_1`  
- `arg_2`  
- `arg_3`  
- `arg_4`  
- `arg_5`  
- `arg_6`  
- `arg_7`..`arg_95`
B.4 PCI Configuration Space  [ia64]

On ia64 processors, the PCI configuration space is handled as fpages. PCI Config fpages can be mapped, granted, and unmapped like memory fpages. Their minimal granularity is 256 (i.e., one single device function). A PCI config fpage of size $2^s$ has a $2^s$-aligned base address $p$, i.e. $p \mod 2^s = 0$. An fpage with base PCI configuration address $p$ and size $2^s$ is denoted as described below.

\[
\text{PCI config fpage } (p, 2^s)
\]

| $p$ (48) | $s'$ (6) | $s = 2^s$ | 0 r w x |

The execute bit of the PCI config fpage is ignored.

---

**Generic Programming Interface**

```
#include <l4/space.h>

Fpage PCIConfigFpage (Word BaseAddress, int FpageSize \geq 256)

Fpage PCIConfigFpageLog2 (Word BaseAddress, int Log2FpageSize < 64)

Delivers a PCI config fpage with the specified location and size.
```
String items can specify cacheability hints to the kernel (see page 52). For ia64, the cacheability hints have the following semantics.

\[
\begin{align*}
hh = 00 & \quad \text{Use the default cacheability strategy. Temporal locality is assumed for all cache levels. That is, cache lines are allocated on all levels for both data read and written.} \\
hh = 01 & \quad \text{No temporal locality is assumed for the first level cache. Temporal locality is assumed for all lower cache levels. That is, cache lines are allocated on all cache levels below L1 for both data read and written.} \\
hh = 10 & \quad \text{No temporal locality is assumed for the first and second level caches. Temporal locality is assumed for all lower cache levels. That is, cache lines are allocated on all cache levels below L2 for both data read and written.} \\
hh = 11 & \quad \text{No temporal locality is assumed on any cache level. That is, cache lines are not allocated on any cache level.}
\end{align*}
\]

Note that support for cacheability hints is processor dependent. Refer to the processor specification to see what type of locality hints the processor supports for load and store instructions.

---

**Convenience Programming Interface**

```c
#include <l4/ipc.h>

CacheAllocationHint UseDefaultCacheLineAllocation
CacheAllocationHint CacheNonTemporalL1
CacheAllocationHint CacheNonTemporalL2
CacheAllocationHint CacheNonTemporalAllLevels
```
B.6 Memory Attributes [ia64]

The ia64 architecture in general supports the following memory attributes values.

<table>
<thead>
<tr>
<th>attribute</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Default</td>
<td>0</td>
</tr>
<tr>
<td>Write Back</td>
<td>1</td>
</tr>
<tr>
<td>Write Coalescing</td>
<td>7</td>
</tr>
<tr>
<td>Uncacheable</td>
<td>5</td>
</tr>
<tr>
<td>Uncacheable Exported</td>
<td>6</td>
</tr>
<tr>
<td>NaT Page</td>
<td>8</td>
</tr>
</tbody>
</table>

Note that some attributes are only supported on certain processors. See the “Intel Itanium Architecture Software Developer’s Manual, Volume 2: System Architecture” for the semantics of the memory attributes.

Generic Programming Interface

```c
#include <l4/misc.h>

Word DefaultMemory
Word WriteBackMemory
Word WriteCoalescingMemory
Word UncacheableMemory
Word UncacheableExportedMemory
Word NaTPageMemory
```
B.7 Memory Descriptors [ia64]

The following memory descriptors (see page 6) are specific to the ia64 architecture.

<table>
<thead>
<tr>
<th>t</th>
<th>type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1</td>
<td>0xF</td>
<td>ACPI Memory</td>
</tr>
</tbody>
</table>

---

Generic Programming Interface

```
#include <l4/kip.h>

Word ACPIMemoryType
```

B.8 Exception Message Format  [ia64]

To be defined.
Appendix C

PowerPC Interface
C.1 Virtual Registers  [powerpc]

Thread Control Registers (TCRs)

TCRs are mapped to memory locations. They are implemented as part of the PowerPC-specific user-level thread control block (UTCB). The address of the current thread’s UTCB is identical to the thread’s local ID, and is thus immutable. The UTCB address is provided in the general purpose register R2 at application start. The R2 register must contain the UTCB address for every system call invocation. UTCBs of other threads must not be accessed, even if they are physically accessible. ThreadWord0 and ThreadWord1 are free to be used by systems software (e.g., IDL compilers). The kernel associates no semantics with these words.

```
<table>
<thead>
<tr>
<th>Address (32)</th>
</tr>
</thead>
<tbody>
<tr>
<td>~ (32)</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>ThreadWord0 (32)</td>
</tr>
<tr>
<td>ThreadWord1 (32)</td>
</tr>
<tr>
<td>VirtualSender/ActualSender (32)</td>
</tr>
<tr>
<td>IntendedReceiver (32)</td>
</tr>
<tr>
<td>XferTimeouts (32)</td>
</tr>
<tr>
<td>ErrorCode (32)</td>
</tr>
<tr>
<td>~ (16)</td>
</tr>
<tr>
<td>copy flags (8)</td>
</tr>
<tr>
<td>preempt flags (8)</td>
</tr>
<tr>
<td>ExceptionHandler (32)</td>
</tr>
<tr>
<td>Pager (32)</td>
</tr>
<tr>
<td>UserDefinedHandle (32)</td>
</tr>
<tr>
<td>ProcessorNo (32)</td>
</tr>
<tr>
<td>MyGlobalId (32)</td>
</tr>
<tr>
<td>MyLocalId = UTCB address (32)</td>
</tr>
</tbody>
</table>
```

The TCR MyLocalId is not part of the UTCB. On PowerPC it is identical with the UTCB address and can be loaded from register R2.

Message Registers (MRs)

Message registers MR_0 through MR_9 map to the processor’s general purpose register file for IPC and LIPC calls. The remaining message registers map to memory locations in the UTCB. MR_10 starts at byte offset 40 in the UTCB, and successive message registers follow in memory.

For the other system calls, message registers map to memory locations in the UTCB, with MR_0 starting at byte offset zero.
Buffer Registers (BRs)

The buffer registers map to memory locations in the UTCB. BR₀ is at byte offset -64 in the UTCB, BR₁ at byte offset -68, etc.

UTCB Memory With Undefined Semantics

The kernel will associate no semantics with memory located at UTCB address...UTCB address + 39. The application can use this memory as thread local storage, e.g., for implementing the L4 API. Note, however, that the memory contents within this region may be overwritten during a system-call operating on message registers.

All undefined UTCB memory which is not covered by the above mentioned region may have kernel defined semantics.
C.2 Systemcalls [powerpc]

The system-calls invoked via the `bl` instruction are located in the kernel’s area of the virtual address space. Their precise locations are stored in the kernel interface page (see page 2). One may invoke the system calls with any instruction that branches to the appropriate target, as long as the link-return register (LR) contains the correct return address.

The locations of the system-calls are fixed during the life of an application. But they may change outside of the life of an application. It is not valid to prelink an application against a set of system call locations. The official locations are always provided in the kip.

The registers defined to survive across system-call invocations (unless otherwise noted) are: R1, R2, R30, R31, and the floating point registers. All other registers contain return values, are undefined, or may be preserved according to processor specific rules.

The R2 register must contain the UTCB pointer when invoking all system calls.

---

**KERNELINTERFACE [Slow Systemcall]**

<table>
<thead>
<tr>
<th>UTCB</th>
<th>R2</th>
<th>– KernelInterface →</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>R3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>R4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>R5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>R6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>R7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>R8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>R9</td>
<td></td>
</tr>
<tr>
<td></td>
<td>R10</td>
<td></td>
</tr>
</tbody>
</table>

For this system-call, all registers other than the output registers are preserved. The tlbia instruction encoding is 0x7c0002e4.

---

**EXCHANGEREGISTERS [Systemcall]**

<table>
<thead>
<tr>
<th>UTCB</th>
<th>R2</th>
<th>– Exchange Registers →</th>
</tr>
</thead>
<tbody>
<tr>
<td>dest</td>
<td>R3</td>
<td></td>
</tr>
<tr>
<td>control</td>
<td>R4</td>
<td></td>
</tr>
<tr>
<td>SP</td>
<td>R5</td>
<td></td>
</tr>
<tr>
<td>IP</td>
<td>R6</td>
<td></td>
</tr>
<tr>
<td>FLAGS</td>
<td>R7</td>
<td></td>
</tr>
<tr>
<td>UserDefinedHandle</td>
<td>R8</td>
<td></td>
</tr>
<tr>
<td>pager</td>
<td>R9</td>
<td></td>
</tr>
<tr>
<td></td>
<td>R10</td>
<td></td>
</tr>
</tbody>
</table>

“FLAGS” refers to the user-modifiable PowerPC processor flags that are held in the MSR register. See the PowerPC Processor Mirroring section (page 125).

---

**THREADCONTROL [Privileged Systemcall]**

<table>
<thead>
<tr>
<th>UTCB</th>
<th>R2</th>
<th>– Thread Control →</th>
</tr>
</thead>
<tbody>
<tr>
<td>dest</td>
<td>R3</td>
<td></td>
</tr>
<tr>
<td>SpaceSpecifier</td>
<td>R4</td>
<td></td>
</tr>
<tr>
<td>Scheduler</td>
<td>R5</td>
<td></td>
</tr>
<tr>
<td>Pager</td>
<td>R6</td>
<td></td>
</tr>
<tr>
<td>UtcbLocation</td>
<td>R7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>R8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>R9</td>
<td></td>
</tr>
<tr>
<td></td>
<td>R10</td>
<td></td>
</tr>
</tbody>
</table>
**SYSTEMCALLS**

---

**SYSTEMCLOCK [Systemcall]**

<table>
<thead>
<tr>
<th>UTCP R2</th>
<th>— R3</th>
<th>— R4</th>
<th>— R5</th>
<th>— R6</th>
<th>— R7</th>
<th>— R8</th>
<th>— R9</th>
<th>— R10</th>
</tr>
</thead>
</table>

→ `SystemClock` →

- `call SystemClock`

R2 ≡

R1 clock 0...31
R4 clock 32...63
R5 ~
R6 ~
R7 ~
R8 ~
R9 ~
R10 ~

---

**THREADSWITCH [Systemcall]**

<table>
<thead>
<tr>
<th>UTCP R2</th>
<th>dest R3</th>
<th>— R4</th>
<th>— R5</th>
<th>— R6</th>
<th>— R7</th>
<th>— R8</th>
<th>— R9</th>
<th>— R10</th>
</tr>
</thead>
</table>

→ `ThreadSwitch` →

- `call ThreadSwitch`

R2 ≡

R1 ~
R4 ~
R5 ~
R6 ~
R7 ~
R8 ~
R9 ~
R10 ~

---

**SCHEDULE [Systemcall]**

<table>
<thead>
<tr>
<th>UTCP R2</th>
<th>dest R3</th>
<th>time control R4</th>
<th>processor control R5</th>
<th>prio R6</th>
<th>preemption control R7</th>
<th>— R8</th>
<th>— R9</th>
<th>— R10</th>
</tr>
</thead>
</table>

→ `Schedule` →

- `call Schedule`

R2 ≡

R3 result
R4 time control
R5 processor control
R6 prio
R7 preemption control
R8 ~
R9 ~
R10 ~

---

**IPC [Systemcall]**

|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

→ `Ipc` →

R0 ≡

R9
R1 ≡
R2 ≡
R3 MR 1
R4 MR 2
R5 MR 3
R6 MR 4
R7 MR 5
R8 MR 6
R9 MR 7
R10 MR 8
R11 ~
R12 ~
R13 ~
R14 MR 0
R14 ~
R15 ~
R16 from
R17 ~
LIPC [Systemcall]

```
| MR_0 | R0 | — Lipc → | R0 | MR_0 |
| — | — | — | — | — |
| R1 | — | R1 → call Lipc |
| R2 | — | — |
| R3 | — | R3 |
| R4 | — | R4 |
| R5 | — | R5 |
| R6 | R6 | R6 |
| R7 | R7 | R7 |
| R8 | R8 | R8 |
| R9 | R9 | R9 |
| R10 | R10 | R10 |
| — | — | — |
| — | — | — |
| — | — | — |
| — | — | — |
| to | R15 | R15 |
| FromSpecifier | R16 | R16 |
| Timeouts | R17 | R17 |
```

UNMAP [Systemcall]

```
| UTCB | R2 | — Unmap → | R2 | — |
| — | — | — | — | — |
| control | R3 | R3 | — | — |
| — | — | R4 | R4 | — |
| — | — | R5 | R5 | — |
| — | — | R6 | R6 | — |
| — | — | R7 | R7 | — |
| — | — | R8 | R8 | — |
| — | — | R9 | R9 | — |
| — | — | R10 | R10 | — |
```

SPACECONTROL [Privileged Systemcall]

```
| UTCB | R2 | — Space Control → | R2 | — |
| SpaceSpecifier | R3 | R3 | — | — |
| control | R4 | R4 | — | — |
| KernelInterfacePageArea | R5 | R5 | — | — |
| UtcbArea | R6 | R6 | — | — |
| Redirector | R7 | R7 | — | — |
| — | — | R8 | R8 | — |
| — | — | R9 | R9 | — |
| — | — | R10 | R10 | — |
```

PROCESSORCONTROL [Privileged Systemcall]

```
| UTCB | R2 | — Processor Control → | R2 | — |
| processor no | R3 | R3 | — | — |
| InternalFreq | R4 | R4 | — | — |
| ExternalFreq | R5 | R5 | — | — |
| voltage | R6 | R6 | — | — |
| — | — | R7 | R7 | — |
| — | — | R8 | R8 | — |
| — | — | R9 | R9 | — |
| — | — | R10 | R10 | — |
```
### Memory Control

**[Privileged Systemcall]**

<table>
<thead>
<tr>
<th>UTCB</th>
<th>R2</th>
<th>Memory Control →</th>
</tr>
</thead>
<tbody>
<tr>
<td>control</td>
<td>R3</td>
<td></td>
</tr>
<tr>
<td>attribute_0</td>
<td>R4</td>
<td></td>
</tr>
<tr>
<td>attribute_1</td>
<td>R5</td>
<td></td>
</tr>
<tr>
<td>attribute_2</td>
<td>R6</td>
<td></td>
</tr>
<tr>
<td>attribute_3</td>
<td>R7</td>
<td></td>
</tr>
<tr>
<td>−</td>
<td>R8</td>
<td></td>
</tr>
<tr>
<td>−</td>
<td>R9</td>
<td></td>
</tr>
<tr>
<td>−</td>
<td>R10</td>
<td></td>
</tr>
</tbody>
</table>

- Memory Control

- call *MemoryControl*

- R2  ≡
- R3  ~
- R4  ~
- R5  ~
- R6  ~
- R7  ~
- R8  ~
- R9  ~
- R10 ~
C.3 Memory Attributes [powerpc]

The PowerPC architecture supports the following memory/cache attribute values, to be used with the MEMORYCONTROL system-call:

<table>
<thead>
<tr>
<th>attribute</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Default</td>
<td>0</td>
</tr>
<tr>
<td>Write-through</td>
<td>1</td>
</tr>
<tr>
<td>Write-back</td>
<td>2</td>
</tr>
<tr>
<td>Caching-inhibited</td>
<td>3</td>
</tr>
<tr>
<td>Caching-enabled</td>
<td>4</td>
</tr>
<tr>
<td>Memory-global (coherent)</td>
<td>5</td>
</tr>
<tr>
<td>Memory-local (not coherent)</td>
<td>6</td>
</tr>
<tr>
<td>Guarded</td>
<td>7</td>
</tr>
<tr>
<td>Speculative</td>
<td>8</td>
</tr>
</tbody>
</table>

The default attributes enable write-back, caching, and speculation. Only if the kernel is compiled with support for multiple processors will memory coherency be enabled by default.

The PowerPC architecture places a variety of restrictions on the usage of the memory/cache attributes. Some combinations are meaningless (such as combining write-through with caching-inhibited), or are not permitted and will lead to undefined behavior (for example, instruction fetching is incompatible with some combinations of attributes). The precise semantics of the memory/cache access attributes are described in the “Programming Environments Manual For 32-Bit Implementations of the PowerPC Architecture.”

Before disabling the cache for a page, the software must ensure that all memory belonging to the target page is flushed from the cache.

---

Generic Programming Interface

#include <l4/misc.h>

Word DefaultMemory
Word WriteThroughMemory
Word WriteBackMemory
Word CachingInhibitedMemory
Word CachingEnabledMemory
Word GlobalMemory
Word LocalMemory
Word GuardedMemory
Word SpeculativeMemory
C.4 Exception Message Format

System Call Trap

System Call Trap Message to Exception Handler

| Flags (32) | MR 12 |
| SP (32)    | MR 11 |
| IP (32)    | MR 10 |
| R0 (32)    | MR 9  |
| R10 (32)   | MR 8  |
| R9 (32)    | MR 7  |
| R8 (32)    | MR 6  |
| R7 (32)    | MR 5  |
| R6 (32)    | MR 4  |
| R5 (32)    | MR 3  |
| R4 (32)    | MR 2  |
| R3 (32)    | MR 1  |
|           | MR 0  |

When user code executes the PowerPC `sc` instruction, the kernel delivers the system call trap message to the exception handler. The kernel preserves only partial user state when handling an `sc` instruction. State is preserved according to the SVR4 PowerPC ABI for function calls. The non-volatile registers are R1, R2, R13…R31, CR2, CR3, CR4, and FPSCR. The volatile registers are R0, R3…R12, CR0, CR1, CR5…CR7, LR, CTR, and XER.

Generic Traps

Generic Trap Message To Exception Handler
Some traps are handled by the kernel and therefore do not generate exception messages.
C.5 Processor Mirroring [powerpc]

The kernel will expose the following supervisor instructions to all user level programs via emulation: MFSPR for the PVR, MFSPR and MTSPR for the DABR and other cpu-specific debug registers.

The kernel will emulate the MFSPR and MTSPR instructions for accessing cpu-specific performance monitor registers on behalf of privileged tasks. The performance monitor registers are global, and not per-thread.

The EXCHANGEREGISTERS system-call accesses the flags of the processor. The flags map directly to the PowerPC MSR register. The following bits may be read and modified by user applications: LE, BE, SE, FE0, and FE1. The kernel also exposes additional cpu-specific bits.
C.6 Booting [powerpc]

Apple New World Compatible Machines

L4 must be loaded into memory at the physical location defined by the kernel’s ELF header. It can be started with virtual addressing enabled or disabled. Execution of L4 must begin at the entry point defined by the kernel’s ELF header.

When entering the kernel, the registers which support in-register file parameter passing, R3–R10 according to the SVR4 ABI, must be cleared for upwards compatibility, except as noted below. All other registers in the register file are undefined at kernel entry.

The kernel may use OpenFirmware for debug console I/O. To support OpenFirmware I/O, the OpenFirmware virtual mode client call-back address must be passed to the kernel in register R5, and OpenFirmware must be prepared to handle client call-backs using virtual addressing. In all other cases, register R5 must be zero.

The boot loader must copy the OpenFirmware device tree to memory, and record its physical location in a memory descriptor of the kernel interface page. The copy of the device tree must include the package handles of the device tree nodes.
Appendix D

Alpha Interface
D.1 Virtual Registers [alpha]

Thread Control Registers (TCRs)

TCRs are mapped to memory locations. They are implemented as part of the Alpha-specific user-level thread control block (UTCB). The address of the current thread’s UTCB is identical to the thread’s local ID, and is thus immutable. The UTCB (and hence local ID) is available through the rdunique PAL call. UTCB objects of the current thread can be accessed as any other memory object. UTCBs of other threads must not be accessed, even if they are physically accessible.

<table>
<thead>
<tr>
<th>Field</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>ThreadWord1 (64)</td>
<td>+88</td>
</tr>
<tr>
<td>ThreadWord0 (64)</td>
<td>+80</td>
</tr>
<tr>
<td>VirtualSender/ActualSender (64)</td>
<td>+72</td>
</tr>
<tr>
<td>IntendedReceiver (64)</td>
<td>+64</td>
</tr>
<tr>
<td>ErrorCode (64)</td>
<td>+56</td>
</tr>
<tr>
<td>XferTimeouts (64)</td>
<td>+48</td>
</tr>
<tr>
<td>~ (48)</td>
<td>+40</td>
</tr>
<tr>
<td>cop flags (8)</td>
<td></td>
</tr>
<tr>
<td>preempt flags (8)</td>
<td></td>
</tr>
<tr>
<td>ExceptionHandler (64)</td>
<td>+32</td>
</tr>
<tr>
<td>Pager (64)</td>
<td>+24</td>
</tr>
<tr>
<td>UserDefinedHandle (64)</td>
<td>+16</td>
</tr>
<tr>
<td>ProcessorNo (64)</td>
<td>+8</td>
</tr>
<tr>
<td>MyGlobalId (64)</td>
<td>← UTCB</td>
</tr>
</tbody>
</table>

MyLocalId = UTCB address (64)
call_pal rdunique

The TCR MyLocalId is not part of the UTCB. On Alpha it is identical with the UTCB address and can be found using the rdunique PAL call.

Message Registers (MRs)

Message registers MR_0 through MR_8 map to the processor’s general purpose register file for IPC and LIPC calls. The remaining message registers map to memory locations in the UTCB. MR_0 starts at byte offset 200 in the UTCB, and successive message registers follow in memory.

For the other system calls, message registers map to memory locations in the UTCB, with MR_0 starting at byte offset 128.
VIRTUAL REGISTERS

**MR** 0...8

<table>
<thead>
<tr>
<th>MR 8</th>
<th>s5</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR 7</td>
<td>s4</td>
</tr>
<tr>
<td>MR 6</td>
<td>s3</td>
</tr>
<tr>
<td>MR 5</td>
<td>s2</td>
</tr>
<tr>
<td>MR 4</td>
<td>s1</td>
</tr>
<tr>
<td>MR 3</td>
<td>s0</td>
</tr>
<tr>
<td>MR 2</td>
<td>t7</td>
</tr>
<tr>
<td>MR 1</td>
<td>t6</td>
</tr>
<tr>
<td>MR 0</td>
<td>s6</td>
</tr>
</tbody>
</table>

**MR** 9...63 [UTCB fields]

| MR 63 (64) | +632 |
| MR 12 (64) | +224 |
| MR 11 (64) | +216 |
| MR 10 (64) | +208 |
| MR 9 (64)  | ←− UTCB address + 200 |

**Buffer Registers (BRs)**

The buffer registers map to memory locations in the UTCB. BR0 is at byte offset 640 in the UTCB, BR1 at byte offset 648, etc.

| BR 32 (64) | +896 |
| BR 1 (64)  | +648 |
| BR 0 (64)  | ←− UTCB address + 640 |

**UTCB Memory With Undefined Semantics**

The kernel will associate no semantics with memory located at UTCB address + 128...UTCB address + 199. The application can use this memory as thread local storage, e.g., for implementing the L4 API. Note, however, that the memory contents within this region may be overwritten during a system-call operating on message registers.

All undefined UTCB memory which is not covered by the above mentioned region may have kernel defined semantics.
D.2 Systemcalls [alpha]

The system-calls invoked via the ‘jsr’ instruction are located in the kernel’s area of the virtual address space. Their precise locations are stored in the kernel interface page (see page 2). One may invoke the system calls with any instruction that branches to the appropriate target, as long as the return-address register (RA) contains the correct return address.

The locations of the system-calls are fixed during the life of an application, although they may change outside of the life of an application. It is not valid to prelink an application against a set of system call locations. The official locations are always provided in the kip.

Unless explicitly stated, the kernel follows the Alpha calling convention for the system call interface. This means that arguments are passed in the a0 – a5 registers and the result is placed in the v0 register. All ‘s’ registers are preserved and all ‘t’ registers are undefined. The sp and ra registers are also preserved.

All floating point registers are preserved across a system call.

All other registers contain return values, are undefined, or may be preserved according to processor specific rules.

---

**KERNEL INTERFACE** [Slow Systemcall]

- v0
  - a0
  - a1
  - a2
  - a3
  - a4
  - a5

---

**EXCHANGE REGISTERS** [Systemcall]

- v0
  - dest
  - control
  - SP
  - IP
  - FLAGS
  - UserDefinedHandle
  - pager
  - t1

---

**THREAD CONTROL** [Privileged Systemcall]

- v0
  - dest
  - SpaceSpecifier
  - Scheduler
  - Pager
  - UtcbLocation
  - a5
**SYSTEMCALLS**

### SYSTEMCALLS

#### SystemCall

- `− v0 | SystemClock → v0 clock`
- `− a0 `~`
- `− a1 `~`
- `− a2 jsr ra, SystemClock`
- `− a3 `~`
- `− a4 `~`
- `− a5 `~`

Note that the SystemClock system call is currently UNIMPLEMENTED on Alpha.

#### ThreadSwitch

- `− v0 | ThreadSwitch → v0 ~`
- `− dest a0 ~`
- `− a1 ~`
- `− a2 jsr ra, ThreadSwitch`
- `− a3 ~`
- `− a4 ~`
- `− a5 ~`

#### Schedule

- `− v0 | Schedule → v0 result`
- `− dest a0 result`
- `− a1 TimeControl`
- `− a2 ProcessorControl`
- `− a3 Priority`
- `− a4 PreemptionControl`
- `− a5 ~`

#### IPC

- `− v0 | Ipc → v0 result`
- `− dest a0 ~`
- `− source a1 ~`
- `− timeout a2 ~`
- `− a3 ~`
- `− a4 ~`
- `− a5 ~`
- `− MR_0 s6 ~`
- `− MR_1 s6 ~`
- `− MR_2 s7 ~`
- `− MR_3 s0 ~`
- `− MR_4 s1 ~`
- `− MR_5 s2 ~`
- `− MR_6 s3 ~`
- `− MR_7 s4 ~`
- `− MR_8 s5 ~`
**LIPC**  
[Systemcall]

<table>
<thead>
<tr>
<th>dest</th>
<th>a0</th>
<th>source</th>
<th>a1</th>
<th>timeout</th>
<th>a2</th>
<th>v0</th>
<th>result</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>a0</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>a1</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>a2</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>a3</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>a4</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>a5</td>
<td>~</td>
</tr>
<tr>
<td>MR_0</td>
<td>s6</td>
<td>MR_1</td>
<td>s6</td>
<td>MR_2</td>
<td>t7</td>
<td>MR_3</td>
<td>s0</td>
</tr>
<tr>
<td>MR_4</td>
<td>s1</td>
<td>MR_5</td>
<td>s2</td>
<td>MR_6</td>
<td>s3</td>
<td>MR_7</td>
<td>s4</td>
</tr>
<tr>
<td>MR_8</td>
<td>s5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MR_0</td>
<td>s6</td>
</tr>
</tbody>
</table>

Note that on Alpha LIPC is not implemented: use IPC instead.

**UNMAP**  
[Systemcall]

<table>
<thead>
<tr>
<th>control</th>
<th>a0</th>
<th>v0</th>
<th>~</th>
</tr>
</thead>
<tbody>
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**SPACECONTROL**  
[Privileged Systemcall]

<table>
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<th>result</th>
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<td>a1</td>
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<td>KIPArea</td>
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<td>a2</td>
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<td>UTCBArea</td>
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</tr>
<tr>
<td>Redirector</td>
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**PROCESSORCONTROL**  
[Privileged Systemcall]

<table>
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<td></td>
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<td>~</td>
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<td>a5</td>
<td>~</td>
</tr>
</tbody>
</table>

Note that on Alpha the ProcessorControl system call is not implemented.
MEMORYCONTROL

[Privileged Systemcall]

| – v0 | – Memory Control → | v0 result |
| – | – | – |
| control | a0 | a0 ~ |
| attribute0 | a1 | a1 ~ |
| attribute1 | a2 | a2 ~ |
| attribute2 | a3 | a3 ~ |
| attribute3 | a4 | a4 ~ |
| – | a5 | a5 ~ |

Note that on Alpha the MemoryControl system call is not implemented: the memory attributes for a page are defined by
the system, and cannot be controlled by the application (or kernel).
D.3 Booting [alpha]

All SRM based machines

L4 must be loaded at the virtual address defined in the ELF header (corresponding to the physical region of the virtual address space). The kernel also requires the bootloader to initialise some kernel data structures, so the supplied bootloader is recommended.

The preferred method for booting the kernel is via BootP. Consult the SRM documentation for instructions on setting up SRM to boot a file from a remote host.
Appendix E

MIPS-64 Interface
E.1 Virtual Registers  [MIPS-64]

Thread Control Registers (TCRs)

TCRs are mapped to memory locations. They are implemented as part of the mips64-specific user-level thread control block (UTCB). The address of the current thread’s UTCB is identical to the thread’s local ID, and is thus immutable. The UTCB (and hence local ID) is available through the break instruction. UTCB objects of the current thread can be accessed as any other memory object. UTCBs of other threads must not be accessed, even if they are physically accessible.

<table>
<thead>
<tr>
<th>ThreadWord 1 (64)</th>
<th>+88</th>
</tr>
</thead>
<tbody>
<tr>
<td>ThreadWord 0 (64)</td>
<td>+80</td>
</tr>
<tr>
<td>VirtualSender/ActualSender (64)</td>
<td>+72</td>
</tr>
<tr>
<td>IntendedReceiver (64)</td>
<td>+64</td>
</tr>
<tr>
<td>ErrorCode (64)</td>
<td>+56</td>
</tr>
<tr>
<td>XferTimeouts (64)</td>
<td>+48</td>
</tr>
<tr>
<td>~ (48)</td>
<td>cop flags (8)</td>
</tr>
<tr>
<td>ExceptionHandler (64)</td>
<td>+32</td>
</tr>
<tr>
<td>Pager (64)</td>
<td>+24</td>
</tr>
<tr>
<td>UserDefinedHandle (64)</td>
<td>+16</td>
</tr>
<tr>
<td>ProcessorNo (64)</td>
<td>+8</td>
</tr>
<tr>
<td>MyGlobalId (64)</td>
<td>← UTCB address</td>
</tr>
</tbody>
</table>

The TCR MyLocalId is not part of the UTCB. On mips64 it is identical with the UTCB address and can be found using the UTCB syscall. The UTCB syscall is a break instruction with an argument of 3 in the AT register. Result is in v0. This is a preliminary solution and going to be changed using a faster access method such as a general purpose register.

Message Registers (MRs)

Message registers MR_0 through MR_7 map to the processor’s general purpose register file for IPC and LIPC calls. The remaining message registers map to memory locations in the UTCB. MR_8 starts at byte offset 192 in the UTCB, and successive message registers follow in memory.

The first eight message registers are mapped to the registers s0 to s7. MR_8...63 are mapped to memory in the UTCB.
**Virtual Registers**

<table>
<thead>
<tr>
<th>MR 0...7</th>
<th></th>
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</thead>
<tbody>
<tr>
<td>MR 0</td>
<td>s0</td>
</tr>
<tr>
<td>MR 1</td>
<td>s1</td>
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<tr>
<td>MR 2</td>
<td>s2</td>
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<tr>
<td>MR 3</td>
<td>s3</td>
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<tr>
<td>MR 4</td>
<td>s4</td>
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<td>MR 5</td>
<td>s5</td>
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<tr>
<td>MR 6</td>
<td>s6</td>
</tr>
<tr>
<td>MR 7</td>
<td>s7</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MR 0...63 [UTCB fields]</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>MR 32 (64)</td>
<td>+896</td>
</tr>
<tr>
<td>:</td>
<td>:</td>
</tr>
<tr>
<td>MR 0 (64)</td>
<td>← UTCB address + 640</td>
</tr>
</tbody>
</table>

**Buffer Registers (BRs)**

The buffer registers map to memory locations in the UTCB. BR 0 is at byte offset 640 in the UTCB, BR 1 at byte offset 648, etc.

<table>
<thead>
<tr>
<th>BR 0...32 [UTCB fields]</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>BR 32 (64)</td>
<td>+896</td>
</tr>
<tr>
<td>:</td>
<td>:</td>
</tr>
<tr>
<td>BR 0 (64)</td>
<td>← UTCB address + 640</td>
</tr>
</tbody>
</table>

**UTCB Memory With Undefined Semantics**

The kernel will associate no semantics with memory located at UTCB address + 128...UTCB address + 191. The application can use this memory as thread local storage, e.g., for implementing the L4 API. Note, however, that the memory contents within this region may be overwritten during a system-call operating on message registers.

All undefined UTCB memory which is not covered by the above mentioned region may have kernel defined semantics.
E.2 Systemcalls [MIPS-64]

The system-calls invoked via the jal instruction are located in the kernel’s area of the virtual address space. Their precise locations are stored in the kernel interface page (see page 2). One may invoke the system calls with any instruction that branches to the appropriate target, as long as the return-address register RA contains the correct return address.

The locations of the system-calls are fixed during the life of an application, although they may change outside of the life of an application. It is not valid to prelink an application against a set of system call locations. The official locations are always provided in the KIP.

In general, the kernel follows the MIPS ABI64 calling convention for the system call boundary. This means that arguments are passed in the a0 – a7 registers, and the result is placed in the v0 register. All floating point registers are preserved across a system call. All other registers contain return values, are undefined, or may be preserved according to processor specific rules.

---

**KERNELINTERFACE** [Slow Systemcall]

<table>
<thead>
<tr>
<th>0x1FACECA114E1F64 at</th>
<th>[KernelInterface ] →</th>
</tr>
</thead>
<tbody>
<tr>
<td>at</td>
<td>[KernelInterface ] →</td>
</tr>
<tr>
<td>v0,v1</td>
<td>[KernelInterface ] →</td>
</tr>
<tr>
<td>a0...a3</td>
<td>[KernelInterface ] →</td>
</tr>
<tr>
<td>t1</td>
<td>[KernelInterface ] →</td>
</tr>
<tr>
<td>t2</td>
<td>[KernelInterface ] →</td>
</tr>
<tr>
<td>t3</td>
<td>[KernelInterface ] →</td>
</tr>
<tr>
<td>t4...t7</td>
<td>[KernelInterface ] →</td>
</tr>
<tr>
<td>t8...t7</td>
<td>[KernelInterface ] →</td>
</tr>
<tr>
<td>gp,sp</td>
<td>[KernelInterface ] →</td>
</tr>
<tr>
<td>ra</td>
<td>[KernelInterface ] →</td>
</tr>
</tbody>
</table>

opcode 0x07FFFFFF

For this system-call, all registers other than the output registers are preserved.

---

**EXCHANGEREGISTERS** [Systemcall]

<table>
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<tr>
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</tr>
<tr>
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<td>[Exchange Registrers ] →</td>
</tr>
<tr>
<td>dest</td>
<td>[Exchange Registrers ] →</td>
</tr>
<tr>
<td>a0</td>
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</tr>
<tr>
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</tr>
<tr>
<td>a1</td>
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<td>a2</td>
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**SYSTEMCALLS**

### THREADCONTROL  [Privileged Systemcall]

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** jal ThreadControl **

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<th>a0</th>
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<th>a2</th>
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<th>a6</th>
<th>a7</th>
<th>a8</th>
<th>a9</th>
<th>sp</th>
<th>ra</th>
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### SYSTEMCLOCK  [Systemcall]

<table>
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<th>a0</th>
<th>a1</th>
<th>a2</th>
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** jal SystemClock **

<table>
<thead>
<tr>
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<th>v1</th>
<th>a0</th>
<th>a1</th>
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### THREADSWITCH  [Systemcall]

<table>
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<th>dest a0</th>
<th>a1</th>
<th>a2</th>
<th>a3</th>
<th>a4</th>
<th>a5</th>
<th>a6</th>
<th>a7</th>
<th>a8</th>
<th>a9</th>
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<th>ra</th>
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<tbody>
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** jal ThreadSwitch **

<table>
<thead>
<tr>
<th>at</th>
<th>v0, v1</th>
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<th>a1</th>
<th>a2</th>
<th>a3</th>
<th>a4</th>
<th>a5</th>
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<th>a9</th>
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<th>ra</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Schedule

**Systemcall**

```
- at
- v0
- v1
  dest v0
time control a1
  processor control a2
  priority a3
  preemption control t0
  t1...13
  t4...17
  t0...17
  t8, t9
  gp
  sp
  s8
  ra
```

** jal Schedule**

```
jal Schedule
  at ~
v0 result
v1 ~
av0 time control
a1 ~
a2 ~
a3 ~
a4 ~
a5...a7 ~
a8...a17 ~
a18, a19 ~
gp ~
sp ~
s8 ~
ra ~
```

### IPC

**Systemcall**

```
- at
- v0
  v1
  MR (0) v1
to a0
  FromSpecifier a1
  Timeouts a2
  a3
  t0...13
  t4...17
  MR x s0
  MR 2 s1
  MR 3 s2
  MR 4 s3
  MR 5 s4
  MR 6 s5
  MR 7 s6
  MR 8 s7
  t8, t9
  gp
  sp
  s8
  ra
```

** jal IPC**

```
jal IPC
  at ~
v0 result
v1 MR (0)
  a0 ~
a1 ~
a2 ~
a3 ~
a4...a7 ~
t4...t7 ~
s0 MR 1
  s1 MR 2
  s2 MR 3
  s3 MR 4
  s4 MR 5
  s5 MR 6
  s6 MR 7
  s7 MR 8
  s8 ~
gp ~
sp ~
s8 ~
ra ~
```
LIPC  [Systemcall]

- at
- v0
- v1
to a0
FromSpecifier a1
Timeouts a2
- a3
- v0...v3
- v4...v7
MR a0
MR a1
MR a2
MR a3
MR a4
MR a5
MR a6
MR a7
- v8, v9
- gp
- sp
- s8
- ra

- Lipc →
- at
- v0
- v1
jal Lipc
- a0
- a1
- a2
- a3
- a4...a7
- s0...s7
- t0...t9
- gp
- sp
- s8
- ra

UNMAP  [Systemcall]

- at
- v0, v1
ccontrol a0
- a1...a3
- v0...v3
- v4...v7
- s0...s7
- v8, v9
- gp
- sp
- s8
- ra

- Unmap →
- at
- v0
- v1
jal Unmap
- a0
- a1...a3
- a4...a7
- s0...s7
- t0...t9
- gp
- sp
- s8
- ra

SPACECONTROL  [Privileged Systemcall]

- at
- v0
- v1
SpaceSpecifier a0
ccontrol a1
KernelInterfacePageArea a2
UtcbArea a3
Redirector a6
- t0...t3
- t4...t7
- s0...s7
- t8, t9
- gp
- sp
- s8
- ra

- Space Control →
- at
- v0
- v1
jal SpaceControl
- a0
- a1...a3
- a4...a7
- t4...t7
- s0...s7
- t8, t9
- gp
- sp
- s8
- ra
### PROCESSOR CONTROL

**[Privileged Systemcall]**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>at</code></td>
<td>Processor no</td>
</tr>
<tr>
<td><code>v0</code></td>
<td><code>InternalFreq</code></td>
</tr>
<tr>
<td><code>v1</code></td>
<td><code>ExternalFreq</code></td>
</tr>
<tr>
<td><code>a0</code></td>
<td><code>voltage</code></td>
</tr>
<tr>
<td><code>a1</code></td>
<td></td>
</tr>
<tr>
<td><code>a2</code></td>
<td></td>
</tr>
<tr>
<td><code>a3</code></td>
<td></td>
</tr>
<tr>
<td><code>t0</code>...<code>t3</code></td>
<td></td>
</tr>
<tr>
<td><code>s4</code>...<code>s7</code></td>
<td></td>
</tr>
<tr>
<td><code>i8</code>, <code>i9</code></td>
<td></td>
</tr>
<tr>
<td><code>gp</code></td>
<td></td>
</tr>
<tr>
<td><code>sp</code></td>
<td></td>
</tr>
<tr>
<td><code>s8</code></td>
<td></td>
</tr>
<tr>
<td><code>ra</code></td>
<td></td>
</tr>
</tbody>
</table>

**Processor Control**

```
jal ProcessorControl
```

### MEMORY CONTROL

**[Privileged Systemcall]**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>at</code></td>
<td>Memory control</td>
</tr>
<tr>
<td><code>v0</code></td>
<td><code>attribute_0</code></td>
</tr>
<tr>
<td><code>v1</code></td>
<td><code>attribute_1</code></td>
</tr>
<tr>
<td><code>a0</code></td>
<td><code>attribute_2</code></td>
</tr>
<tr>
<td><code>a1</code></td>
<td><code>attribute_3</code></td>
</tr>
<tr>
<td><code>a2</code></td>
<td></td>
</tr>
<tr>
<td><code>a3</code></td>
<td></td>
</tr>
<tr>
<td><code>a4</code></td>
<td></td>
</tr>
<tr>
<td><code>a5</code>...<code>a7</code></td>
<td></td>
</tr>
<tr>
<td><code>t4</code>...<code>t7</code></td>
<td></td>
</tr>
<tr>
<td><code>s8</code></td>
<td></td>
</tr>
<tr>
<td><code>gp</code></td>
<td></td>
</tr>
<tr>
<td><code>sp</code></td>
<td></td>
</tr>
<tr>
<td><code>ra</code></td>
<td></td>
</tr>
</tbody>
</table>

**Memory Control**

```
jal MemoryControl
```
The mips64 architecture supports the following memory/cache attribute values, to be used with the `MEMORYCONTROL` system-call:

<table>
<thead>
<tr>
<th>attribute</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Default</td>
<td>0</td>
</tr>
<tr>
<td>Uncached</td>
<td>1</td>
</tr>
<tr>
<td>Write-back</td>
<td>2</td>
</tr>
<tr>
<td>Write-through</td>
<td>3</td>
</tr>
<tr>
<td>Write-through (no allocate)</td>
<td>4</td>
</tr>
<tr>
<td>Flush (Cache flush)</td>
<td>31</td>
</tr>
</tbody>
</table>

The default attributes depend on the platform and not all modes are defined for all processors.

Before disabling the cache for a page, the software must ensure that all memory belonging to the target page is flushed from the cache.
E.4 Booting  [MIPS-64]

The kernel is provided as an ELF file and must be loaded according to the load addresses defined in the ELF header (corresponding to the physical region of the virtual address space). The kernel must be started in 64bit mode.
Appendix F

AMD64 Interface
F.1 Virtual Registers  [amd64]

Thread Control Registers (TCRs)

TCRs are implemented as part of the amd64-specific user-level thread control block (UTCB). The address of the current thread’s UTCB will not change over the lifetime of the thread. Setting the UTCB address of an active thread via THREADCONTROL is similar to deletion and re-creation. There is a fixed correlation between the UtcbLocation parameter when invoking THREADCONTROL and the UTCB address. The UTCB address of the current thread can be loaded through a machine instruction

\[
\text{mov} \quad \%gs:[0], \%r
\]

UTCB objects of the current thread can then be accessed as any other memory object. UTCBs of other threads must not be accessed, even if they are physically accessible. ThreadWord0 and ThreadWord1 are free to be used by systems software (e.g., IDL compilers). The kernel associates no semantics with these words.

<table>
<thead>
<tr>
<th>ThreadWord0 (64)</th>
<th>← UTCB address – 32</th>
</tr>
</thead>
<tbody>
<tr>
<td>ThreadWord1 (64)</td>
<td>– 40</td>
</tr>
<tr>
<td>VirtualSender/ActualSender (64)</td>
<td>– 48</td>
</tr>
<tr>
<td>IntendedReceiver (64)</td>
<td>– 56</td>
</tr>
<tr>
<td>XferTimeouts (64)</td>
<td>– 64</td>
</tr>
<tr>
<td>ErrorCode (64)</td>
<td>– 72</td>
</tr>
<tr>
<td>~ (48)</td>
<td>cop flags (8)</td>
</tr>
<tr>
<td>ExceptionHandler (64)</td>
<td>– 88</td>
</tr>
<tr>
<td>Pager (64)</td>
<td>– 96</td>
</tr>
<tr>
<td>UserDefinedHandle (64)</td>
<td>–104</td>
</tr>
<tr>
<td>ProcessorNo (64)</td>
<td>–112</td>
</tr>
<tr>
<td>MyGlobalId (64)</td>
<td>–120</td>
</tr>
</tbody>
</table>

\[
\begin{align*}
\text{MyLocalId} &= \text{UTCB address} (64) \\
\text{gs:}[0] &\end{align*}
\]

The TCR MyLocalId is not part of the UTCB. On amd64 it is identical with the UTCB address and can be loaded from memory location gs:0.

Message Registers (MRs)

Memory-mapped MRs are implemented as part of the ia32-specific user-level thread control block (UTCB). The address of the current thread’s UTCB will not change over the lifetime of the thread. Setting the UTCB address of an active thread via THREADCONTROL is similar to deletion and re-creation. There is a fixed correlation between the UtcbLocation parameter when invoking THREADCONTROL and the UTCB address. The UTCB address of the current thread can be
VIRTUAL REGISTERS

loaded through a machine instruction

\[
\text{mov \hspace{1em} \%gs:[0], \%r}
\]

UTCB objects of the current thread can then be accessed as any other memory object. UTCBs of other threads must not be accessed, even if they are physically accessible.

The first 8 message registers MR 0 through MR 7 are always mapped to general register. MR 8...63 are always mapped to memory.

\[
\begin{array}{|c|c|}
\hline
MR 0...7 & \\
\hline
MR 7 & R15 \\
MR 6 & R14 \\
MR 5 & R13 \\
MR 4 & R12 \\
MR 3 & R10 \\
MR 2 & RBX \\
MR 1 & RAX \\
MR 0 & R09 \\
\hline
\end{array}
\]

\[
\begin{array}{|c|c|}
\hline
MR 1...63 & \text{[UTCB fields]} \\
\hline
MR 63 (64) & + 456 \\
MR 10 (64) & + 80 \\
MR 9 (64) & + 72 \\
MR 8 (64) & \text{UTCB address + 64} \\
\hline
\end{array}
\]

Buffer Registers (BRs)

BRs are implemented as part of the ia32-specific user-level thread control block (UTCB). The address of the current thread’s UTCB will not change over the lifetime of the thread. Setting the UTCB address of an active thread via THREAD-CONTROL is similar to deletion and re-creation. There is a fixed correlation between the UtcbLocation parameter when invoking THREADCONTROL and the UTCB address. The UTCB address of the current thread can be loaded through a machine instruction

\[
\text{mov \hspace{1em} \%gs:[0], \%r}
\]

UTCB objects of the current thread can then be accessed as any other memory object. UTCBs of other threads must not be accessed, even if they are physically accessible.

\[
\begin{array}{|c|c|}
\hline
BR 0...32 & \text{[UTCB fields]} \\
\hline
\end{array}
\]
<table>
<thead>
<tr>
<th>Virtual Register (64)</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>BR_0</td>
<td>UCB address –128</td>
</tr>
<tr>
<td>BR_1</td>
<td>–136</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>BR_32</td>
<td>–384</td>
</tr>
</tbody>
</table>
F.2 Systemcalls [amd64]

The system-calls which are invoked by the call instruction take the target of the calls the from system-call link fields in the kernel interface page (see page 2). Each system-call link specifies an address relative to the kernel interface page’s base address. An application may use instructions other than call to invoke the system-calls, but must ensure that a valid return address resides on the stack.

<table>
<thead>
<tr>
<th>KernelInterface [Slow Systemcall]</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAX</td>
</tr>
<tr>
<td>lock: nop</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ExchangeRegisters [Systemcall]</th>
</tr>
</thead>
<tbody>
<tr>
<td>dest</td>
</tr>
<tr>
<td>SP control pager</td>
</tr>
<tr>
<td>IP</td>
</tr>
<tr>
<td>UserDefinedHandle</td>
</tr>
</tbody>
</table>

“FLAGS” refers to the user-modifiable amd64 processor flags that are held in the RFLAGS register.
### Thread Control

<table>
<thead>
<tr>
<th>Privileged Systemcall</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>Thread Control</code></td>
</tr>
<tr>
<td><code>call ThreadControl</code></td>
</tr>
<tr>
<td><code>− RAX</code></td>
</tr>
<tr>
<td><code>− RCX</code></td>
</tr>
<tr>
<td><code>− RDX</code></td>
</tr>
<tr>
<td><code>− RSI</code></td>
</tr>
<tr>
<td><code>− RDI</code></td>
</tr>
<tr>
<td><code>− RBX</code></td>
</tr>
<tr>
<td><code>− RBP</code></td>
</tr>
<tr>
<td><code>− R08</code></td>
</tr>
<tr>
<td><code>− R09</code></td>
</tr>
<tr>
<td><code>− R10</code></td>
</tr>
<tr>
<td><code>− R11</code></td>
</tr>
<tr>
<td><code>− R12</code></td>
</tr>
<tr>
<td><code>− R13</code></td>
</tr>
<tr>
<td><code>− R14</code></td>
</tr>
<tr>
<td><code>− R15</code></td>
</tr>
<tr>
<td><code>− RSP</code></td>
</tr>
</tbody>
</table>

### System Clock

<table>
<thead>
<tr>
<th>Systemcall</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>SystemClock</code></td>
</tr>
<tr>
<td><code>call SystemClock</code></td>
</tr>
<tr>
<td><code>− RAX</code></td>
</tr>
<tr>
<td><code>− RCX</code></td>
</tr>
<tr>
<td><code>− RDX</code></td>
</tr>
<tr>
<td><code>− RSI</code></td>
</tr>
<tr>
<td><code>− RDI</code></td>
</tr>
<tr>
<td><code>− RBX</code></td>
</tr>
<tr>
<td><code>− RBP</code></td>
</tr>
<tr>
<td><code>− R08</code></td>
</tr>
<tr>
<td><code>− R09</code></td>
</tr>
<tr>
<td><code>− R10</code></td>
</tr>
<tr>
<td><code>− R11</code></td>
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<tr>
<td><code>− R12</code></td>
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<tr>
<td><code>− R13</code></td>
</tr>
<tr>
<td><code>− R14</code></td>
</tr>
<tr>
<td><code>− R15</code></td>
</tr>
<tr>
<td><code>− RSP</code></td>
</tr>
</tbody>
</table>

### Thread Switch

<table>
<thead>
<tr>
<th>Systemcall</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>ThreadSwitch</code></td>
</tr>
<tr>
<td><code>call ThreadSwitch</code></td>
</tr>
<tr>
<td><code>− RAX</code></td>
</tr>
<tr>
<td><code>− RCX</code></td>
</tr>
<tr>
<td><code>− RDX</code></td>
</tr>
<tr>
<td><code>− RSI</code></td>
</tr>
<tr>
<td><code>− RDI</code></td>
</tr>
<tr>
<td><code>− RBX</code></td>
</tr>
<tr>
<td><code>− RBP</code></td>
</tr>
<tr>
<td><code>− R08</code></td>
</tr>
<tr>
<td><code>− R09</code></td>
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<tr>
<td><code>− R10</code></td>
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<tr>
<td><code>− R11</code></td>
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<tr>
<td><code>− R12</code></td>
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<td><code>− R14</code></td>
</tr>
<tr>
<td><code>− R15</code></td>
</tr>
<tr>
<td><code>− RSP</code></td>
</tr>
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</table>
### SCHEDULE [Systemcall]

<table>
<thead>
<tr>
<th></th>
<th>– Schedule →</th>
<th>RAX</th>
<th>RAX</th>
<th>time control</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>– Schedule</td>
<td>RCX</td>
<td>RCX</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>time control</td>
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<td>RDX</td>
<td>~</td>
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<td>prior</td>
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<td>RSI</td>
<td>~</td>
</tr>
<tr>
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<td>dest</td>
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<td>RBX</td>
<td>RBX</td>
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<td></td>
<td>RBP</td>
<td>RBP</td>
<td>~</td>
</tr>
<tr>
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</tr>
<tr>
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<td>control</td>
<td>R09</td>
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<td></td>
<td>R10</td>
<td>R10</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R11</td>
<td>R11</td>
<td>~</td>
</tr>
<tr>
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<td>R12</td>
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<td>~</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RSP</td>
<td>RSP</td>
<td>~</td>
</tr>
</tbody>
</table>

### IPC [Systemcall]

<table>
<thead>
<tr>
<th></th>
<th>– Ipc →</th>
<th>RAX</th>
<th>RAX</th>
<th>MR 1</th>
</tr>
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<tbody>
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<td>– Ipc</td>
<td>RCX</td>
<td>RCX</td>
<td>~</td>
</tr>
<tr>
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<td>FromSpecifier</td>
<td>RDX</td>
<td>RDX</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>to</td>
<td>RSI</td>
<td>RSI</td>
<td>from</td>
</tr>
<tr>
<td></td>
<td>UTCB</td>
<td>RDI</td>
<td>RDI</td>
<td>~</td>
</tr>
<tr>
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<td>MR 2</td>
<td>RBX</td>
<td>RBX</td>
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</tr>
<tr>
<td></td>
<td>–</td>
<td>RBP</td>
<td>RBP</td>
<td>~</td>
</tr>
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<td></td>
<td>Timeouts</td>
<td>R08</td>
<td>R08</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>MR 0</td>
<td>R09</td>
<td>R09</td>
<td>MR 0</td>
</tr>
<tr>
<td></td>
<td>MR 1</td>
<td>R10</td>
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<tr>
<td></td>
<td>MR 2</td>
<td>R11</td>
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<td>~</td>
</tr>
<tr>
<td></td>
<td>MR 3</td>
<td>R12</td>
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<td>~</td>
</tr>
<tr>
<td></td>
<td>MR 4</td>
<td>R13</td>
<td>R13</td>
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</tr>
<tr>
<td></td>
<td>MR 5</td>
<td>R14</td>
<td>R14</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>MR 6</td>
<td>R15</td>
<td>R15</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>MR 7</td>
<td>R15</td>
<td>R15</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>–</td>
<td>RSP</td>
<td>RSP</td>
<td>~</td>
</tr>
</tbody>
</table>

### LIPC [Systemcall]

<table>
<thead>
<tr>
<th></th>
<th>– Lipc →</th>
<th>RAX</th>
<th>RAX</th>
<th>MR 1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>– Lipc</td>
<td>RCX</td>
<td>RCX</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>FromSpecifier</td>
<td>RDX</td>
<td>RDX</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>to</td>
<td>RSI</td>
<td>RSI</td>
<td>from</td>
</tr>
<tr>
<td></td>
<td>UTCB</td>
<td>RDI</td>
<td>RDI</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>MR 2</td>
<td>RBX</td>
<td>RBX</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>–</td>
<td>RBP</td>
<td>RBP</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>Timeouts</td>
<td>R08</td>
<td>R08</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>MR 0</td>
<td>R09</td>
<td>R09</td>
<td>MR 0</td>
</tr>
<tr>
<td></td>
<td>MR 1</td>
<td>R10</td>
<td>R10</td>
<td>MR 1</td>
</tr>
<tr>
<td></td>
<td>MR 2</td>
<td>R11</td>
<td>R11</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>MR 3</td>
<td>R12</td>
<td>R12</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>MR 4</td>
<td>R13</td>
<td>R13</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>MR 5</td>
<td>R14</td>
<td>R14</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>MR 6</td>
<td>R15</td>
<td>R15</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>MR 7</td>
<td>R15</td>
<td>R15</td>
<td>~</td>
</tr>
<tr>
<td></td>
<td>–</td>
<td>RSP</td>
<td>RSP</td>
<td>~</td>
</tr>
</tbody>
</table>
### UNMAP [Systemcall]

<table>
<thead>
<tr>
<th></th>
<th>Unmap →</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>RAX</td>
<td></td>
<td>RAX</td>
<td>~</td>
</tr>
<tr>
<td>RCX</td>
<td></td>
<td>RCX</td>
<td>~</td>
</tr>
<tr>
<td>RDX MRO</td>
<td></td>
<td>RDX</td>
<td>~</td>
</tr>
<tr>
<td>RSI</td>
<td></td>
<td>RSI</td>
<td>~</td>
</tr>
<tr>
<td>RDI</td>
<td></td>
<td>RDI</td>
<td>~</td>
</tr>
<tr>
<td>RBX</td>
<td></td>
<td>RBX</td>
<td>~</td>
</tr>
<tr>
<td>RBP</td>
<td></td>
<td>RBP</td>
<td>~</td>
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<tr>
<td>R08</td>
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<td>R08</td>
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<td>R09</td>
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<td>R10</td>
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<td>R11</td>
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<td>R12</td>
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<td>R13</td>
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<td>R14</td>
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<td>R15</td>
<td></td>
<td>R15</td>
<td>~</td>
</tr>
<tr>
<td>RSP</td>
<td></td>
<td>RSP</td>
<td>~</td>
</tr>
</tbody>
</table>

### SPACE CONTROL [Privileged Systemcall]

<table>
<thead>
<tr>
<th></th>
<th>Space Control →</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>RAX</td>
<td>result</td>
<td>RAX</td>
<td>~</td>
</tr>
<tr>
<td>RCX</td>
<td></td>
<td>RCX</td>
<td>~</td>
</tr>
<tr>
<td>RDX</td>
<td>control</td>
<td>RDX</td>
<td>~</td>
</tr>
<tr>
<td>RSI</td>
<td></td>
<td>RSI</td>
<td>~</td>
</tr>
<tr>
<td>RDI</td>
<td></td>
<td>RDI</td>
<td>~</td>
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<tr>
<td>RBX</td>
<td></td>
<td>RBX</td>
<td>~</td>
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<tr>
<td>RBP</td>
<td></td>
<td>RBP</td>
<td>~</td>
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<tr>
<td>R08</td>
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<td>R08</td>
<td>~</td>
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<td>R09</td>
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<td>R09</td>
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<td>R10</td>
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<td>R10</td>
<td>~</td>
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<tr>
<td>R11</td>
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<td>R11</td>
<td>~</td>
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<td>R12</td>
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<td>R13</td>
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<td>R14</td>
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<td>R15</td>
<td></td>
<td>R15</td>
<td>~</td>
</tr>
<tr>
<td>RSP</td>
<td></td>
<td>RSP</td>
<td>~</td>
</tr>
</tbody>
</table>

### PROCESSOR CONTROL [Privileged Systemcall]

<table>
<thead>
<tr>
<th></th>
<th>Processor Control →</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>RAX</td>
<td>result</td>
<td>RAX</td>
<td>~</td>
</tr>
<tr>
<td>RCX</td>
<td></td>
<td>RCX</td>
<td>~</td>
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<tr>
<td>RDX</td>
<td></td>
<td>RDX</td>
<td>~</td>
</tr>
<tr>
<td>RSI</td>
<td></td>
<td>RSI</td>
<td>~</td>
</tr>
<tr>
<td>RDI</td>
<td></td>
<td>RDI</td>
<td>~</td>
</tr>
<tr>
<td>RBX</td>
<td></td>
<td>RBX</td>
<td>~</td>
</tr>
<tr>
<td>RBP</td>
<td></td>
<td>RBP</td>
<td>~</td>
</tr>
<tr>
<td>R08</td>
<td></td>
<td>R08</td>
<td>~</td>
</tr>
<tr>
<td>R09</td>
<td></td>
<td>R09</td>
<td>~</td>
</tr>
<tr>
<td>R10</td>
<td></td>
<td>R10</td>
<td>~</td>
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<tr>
<td>R11</td>
<td></td>
<td>R11</td>
<td>~</td>
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<td>R12</td>
<td></td>
<td>R12</td>
<td>~</td>
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<td>R13</td>
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<td>R13</td>
<td>~</td>
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<td>R14</td>
<td></td>
<td>R14</td>
<td>~</td>
</tr>
<tr>
<td>R15</td>
<td></td>
<td>R15</td>
<td>~</td>
</tr>
<tr>
<td>RSP</td>
<td></td>
<td>RSP</td>
<td>~</td>
</tr>
</tbody>
</table>
### Memory Control

<table>
<thead>
<tr>
<th>attribute&lt;sub&gt;3&lt;/sub&gt;</th>
<th>RAX</th>
<th>Memory Control</th>
<th>RAX</th>
<th>result</th>
</tr>
</thead>
<tbody>
<tr>
<td>−</td>
<td>RCX</td>
<td>call MemoryControl</td>
<td>RCX</td>
<td>~</td>
</tr>
<tr>
<td>attribute&lt;sub&gt;0&lt;/sub&gt;</td>
<td>RDX</td>
<td></td>
<td>RDX</td>
<td>~</td>
</tr>
<tr>
<td>control</td>
<td>RSI</td>
<td></td>
<td>RSI</td>
<td>~</td>
</tr>
<tr>
<td>UTCB</td>
<td>RDI</td>
<td></td>
<td>RDI</td>
<td>~</td>
</tr>
<tr>
<td>−</td>
<td>RBX</td>
<td></td>
<td>RBX</td>
<td>~</td>
</tr>
<tr>
<td>−</td>
<td>RBP</td>
<td></td>
<td>RBP</td>
<td>~</td>
</tr>
<tr>
<td>attribute&lt;sub&gt;1&lt;/sub&gt;</td>
<td>R08</td>
<td></td>
<td>R08</td>
<td>~</td>
</tr>
<tr>
<td>attribute&lt;sub&gt;2&lt;/sub&gt;</td>
<td>R09</td>
<td></td>
<td>R09</td>
<td>~</td>
</tr>
<tr>
<td>−</td>
<td>R10</td>
<td></td>
<td>R10</td>
<td>~</td>
</tr>
<tr>
<td>−</td>
<td>R11</td>
<td></td>
<td>R11</td>
<td>~</td>
</tr>
<tr>
<td>−</td>
<td>R12</td>
<td></td>
<td>R12</td>
<td>~</td>
</tr>
<tr>
<td>−</td>
<td>R13</td>
<td></td>
<td>R13</td>
<td>~</td>
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<tr>
<td>−</td>
<td>R14</td>
<td></td>
<td>R14</td>
<td>~</td>
</tr>
<tr>
<td>−</td>
<td>R15</td>
<td></td>
<td>R15</td>
<td>~</td>
</tr>
<tr>
<td>−</td>
<td>RSP</td>
<td></td>
<td>RSP</td>
<td>~</td>
</tr>
</tbody>
</table>
F.3 IO-Ports [amd64]

On AMD64 processors, IO-ports are handled as fpages. IO fpages can be mapped, granted, and unmapped like memory fpages. Their minimal granularity is 1. An IO-fpage of size $2^s$ has a $2^s$-aligned base address $p$, i.e. $p \mod 2^s = 0$. An fpage with base port address $p$ and size $2^s$ is denoted as described below.

$$IO\ fpage\ (p, 2^s)$$

\[
\begin{array}{|c|c|c|c|}
\hline
\text{p (16/48)} & s' (6) & s = 2 (6) & 0 \ r \ w \ x \\
\hline
\end{array}
\]

IO-ports can only be mapped idempotently, i.e., physical port $x$ is either mapped at IO address $x$ in the task’s IO address space, or it is not mapped at all.

---

Generic Programming Interface

```
#include <l4/space.h>

Fpage IoFpage (Word BaseAddress, int FpageSize)
Fpage IoFpageLog2 (Word BaseAddress, int Log2FpageSize < 64)
```

Delivers an IO fpage with the specified location and size.
F.4 Cacheability Hints

String items can specify cacheability hints to the kernel (see page 52). For amd64, the cacheability hints have the following semantics.

- $hh = 00$: Use the processor’s default cacheability strategy. Typically, cache lines are allocated for data read and written (assuming that the processor’s default strategy is write-back and write-allocate).
- $hh = 01$: Allocate cache lines in the entire cache hierarchy for data read or written.
- $hh = 10$: Do not allocate new cache lines (entire cache hierarchy) for data read or written.
- $hh = 11$: Allocate only new L1 cache line for data read or written. Do not allocate cache lines in lower cache hierarchies.

Convenience Programming Interface

```c
#include <l4/ipc.h>

CacheAllocationHint UseDefaultCacheLineAllocation
CacheAllocationHint AllocateNewCacheLines
CacheAllocationHint DoNotAllocateNewCacheLines
CacheAllocationHint AllocateOnlyNewL1CacheLines
```
F.5 Memory Attributes  [amd64]

The AMD64 architecture in general supports the following memory attributes values.

<table>
<thead>
<tr>
<th>attribute</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Default</td>
<td>0</td>
</tr>
<tr>
<td>Uncacheable</td>
<td>1</td>
</tr>
<tr>
<td>Write Combining</td>
<td>2</td>
</tr>
<tr>
<td>Write Through</td>
<td>5</td>
</tr>
<tr>
<td>Write Protected</td>
<td>6</td>
</tr>
<tr>
<td>Write Back</td>
<td>7</td>
</tr>
</tbody>
</table>

Note that some attributes are only supported on certain processors. See the “AMD64 Architecture Programmer’s Manual Volume 2: System Programming” for the semantics of the memory attributes and which processors they are supported on.

Generic Programming Interface

#include <l4/misc.h>

Word DefaultMemory
Word UncacheableMemory
Word WriteCombiningMemory
Word WriteThroughMemory
Word WriteProtectedMemory
Word WriteBackMemory
### F.6 Exception Message Format

<table>
<thead>
<tr>
<th>RFLAGS</th>
<th>MR 18</th>
</tr>
</thead>
<tbody>
<tr>
<td>RSP</td>
<td>MR 17</td>
</tr>
<tr>
<td>R11</td>
<td>MR 16</td>
</tr>
<tr>
<td>R09</td>
<td>MR 15</td>
</tr>
<tr>
<td>R08</td>
<td>MR 14</td>
</tr>
<tr>
<td>RBP</td>
<td>MR 13</td>
</tr>
<tr>
<td>RDI</td>
<td>MR 12</td>
</tr>
<tr>
<td>RSI</td>
<td>MR 11</td>
</tr>
<tr>
<td>RDX</td>
<td>MR 10</td>
</tr>
<tr>
<td>RCX</td>
<td>MR  9</td>
</tr>
<tr>
<td>RAX</td>
<td>MR  8</td>
</tr>
<tr>
<td>R15</td>
<td>MR  7</td>
</tr>
<tr>
<td>R14</td>
<td>MR  6</td>
</tr>
<tr>
<td>R13</td>
<td>MR  5</td>
</tr>
<tr>
<td>R12</td>
<td>MR  4</td>
</tr>
<tr>
<td>R10</td>
<td>MR  3</td>
</tr>
<tr>
<td>RBX</td>
<td>MR  2</td>
</tr>
<tr>
<td>RIP</td>
<td>MR  1</td>
</tr>
<tr>
<td>−4/−5</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>t = 0</td>
<td>u = 18</td>
</tr>
</tbody>
</table>

#PF (page fault), #MC (machine check exception), and some #GP (general protection), #SS (stack segment fault), and #NM (no math coprocessor) exceptions are handled by the kernel and therefore do not generate exception messages.

Note that executing an INT \( n \) instructions in 32-bit mode will always raise a #GP (general protection). The exception handler may interpret the error code \( 8n + 2 \), see processor manual) and emulate the INT \( n \) accordingly.
Segments

L4 uses a flat (unsegmented) memory model. There are only three segments available: `user_space`, a read/write segment, `user_space_exec`, an executable segment, and `utcb_address`, a read-only segment. Both `user_space` and `user_space_exec` cover (at least) the complete user-level address space. `Utcb_address` covers only enough memory to hold the UTCB address.

The values of segment selectors are undefined. When a thread is created, its segment registers SS, DS, ES and FS are initialized with `user_space`, GS with `utcb_address`, and CS with `user_space_exec`. Whenever the kernel detects a general protection exception and the segment registers are not loaded properly, it reloads them with the above mentioned selectors. From the user’s point of view, the segment registers cannot be modified.

However, the binary representation of `user_space` and `user_space_exec` may change at any point during program execution. Never rely on any particular value.

Furthermore, the LSL (load segment limit) machine instruction may deliver wrong segment limits, even floating ones. The result of this instruction is always undefined.

Debug Registers

User-level debug registers exist per thread. DR0…3, DR6 and DR7 can be accessed by the machine instructions `mov n,DRx` and `mov DRx,r`. However, only task-local breakpoints can be activated, i.e., bits G0…3 in DR7 cannot be set. Breakpoints operate per thread. Breakpoints are signaled as #DB exception (INT 1).

Note that user-level breakpoints are suspended when kernel breakpoints are set by the kernel debugger.

Model-Specific Registers

All privileged threads in the system have read and write access to all the Model-Specific Registers (MSRs) of the CPU. Modification of some MSRs may lead to undefined system behavior. Any access to an MSR by an unprivileged thread will raise an exception.
F.8 Booting

PC-compatible Machines

L4 can be loaded at any 16-byte-aligned location beyond 0x1000 in physical memory. It can be started in real mode or in 32-bit protected mode at address 0x100 or 0x1000 relative to its load address. The protected-mode conditions are compliant to the Multiboot Standard Version 0.6.

<table>
<thead>
<tr>
<th>Start Preconditions</th>
<th>Real Mode</th>
<th>32-bit Protected Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>load base ((L))</td>
<td>(L \geq 0x1000), 16-byte aligned</td>
<td>(L \geq 0x1000)</td>
</tr>
<tr>
<td>load offset ((X))</td>
<td>(X = 0x100) or (X = 0x1000)</td>
<td>(X = 0x100) or (X = 0x1000)</td>
</tr>
<tr>
<td>Interrupts</td>
<td>disabled</td>
<td>disabled</td>
</tr>
<tr>
<td>Gate A20</td>
<td>(\sim)</td>
<td>open</td>
</tr>
<tr>
<td>EFLAGS</td>
<td>(I=0)</td>
<td>(I=0), (VM=0)</td>
</tr>
<tr>
<td>CR0</td>
<td>PE=0</td>
<td>PE=1, PG=0</td>
</tr>
<tr>
<td>(E)IP</td>
<td>(X)</td>
<td>(L + X)</td>
</tr>
<tr>
<td>CS</td>
<td>(L/16)</td>
<td>0, 4GB, 32-bit exec</td>
</tr>
<tr>
<td>SS, DS, ES</td>
<td>(\sim)</td>
<td>0, 4GB, read/write</td>
</tr>
<tr>
<td>EAX</td>
<td>(\sim)</td>
<td>0x2BADB002</td>
</tr>
<tr>
<td>EBX</td>
<td>(\sim)</td>
<td>(\sim)</td>
</tr>
<tr>
<td>((P + 0))</td>
<td>n/a</td>
<td>(\sim) or 1</td>
</tr>
<tr>
<td>((P + 4))</td>
<td></td>
<td>below 640 K mem in K</td>
</tr>
<tr>
<td>((P + 8))</td>
<td></td>
<td>beyond 1M mem in K</td>
</tr>
<tr>
<td>all remaining registers &amp; flags</td>
<td>(\sim)</td>
<td>(\sim)</td>
</tr>
<tr>
<td>(general, floating point, ESP, xDT, TR, CRx, DRx)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

L4 relocates itself to 0x1000, enters protected mode if started in real mode, enables paging and initializes itself.
Appendix G

SPARC v9 Interface
G.1 Virtual Registers  [SPARC v9]

Thread Control Registers (TCRs)
TCRs are mapped to memory locations. They are implemented as part of the sparc64-specific user-level thread control block (UTCB). The address of the current thread’s UTCB is identical to the thread’s local ID, and is thus immutable. Setting the UTCB address of an active thread via THREADCONTROL is similar to deletion and re-creation. There is a fixed correlation between the UtcbLocation parameter when invoking THREADCONTROL and the UTCB address. The UTCB address is provided in the general purpose register g7 at application start. UTCB objects of the current thread can then be accessed as any other memory object. UTCBs of other threads must not be accessed, even if they are physically accessible. ThreadWord0 and ThreadWord1 are free to be used by systems software (e.g., IDL compilers). The kernel associates no semantics with these words.

<table>
<thead>
<tr>
<th>Address Offset</th>
<th>Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>+ 80</td>
<td>ThreadWord0 [64]</td>
</tr>
<tr>
<td>+ 88</td>
<td>ThreadWord1 [64]</td>
</tr>
<tr>
<td>+ 88</td>
<td>~ (48)</td>
</tr>
<tr>
<td>+ 72</td>
<td>cop flags (8)</td>
</tr>
<tr>
<td>+ 72</td>
<td>preempt flags (8)</td>
</tr>
<tr>
<td>+ 64</td>
<td>ProcessorNo [64]</td>
</tr>
<tr>
<td>+ 56</td>
<td>VirtualSender/ActualSender [64]</td>
</tr>
<tr>
<td>+ 48</td>
<td>IntendedReceiver [64]</td>
</tr>
<tr>
<td>+ 40</td>
<td>ErrorCode [64]</td>
</tr>
<tr>
<td>+ 32</td>
<td>XferTimeouts [64]</td>
</tr>
<tr>
<td>+ 24</td>
<td>UserDefinedHandle [64]</td>
</tr>
<tr>
<td>+ 16</td>
<td>ExceptionHandler [64]</td>
</tr>
<tr>
<td>+ 8</td>
<td>Pager [64]</td>
</tr>
<tr>
<td>←− UTCB address</td>
<td>MyGlobalId [64]</td>
</tr>
<tr>
<td>g7</td>
<td>MyLocalId = UTCB address [64]</td>
</tr>
</tbody>
</table>

The TCR MyLocalId is not part of the UTCB. On SPARC v9 it is identical with the UTCB address and can be loaded from register g7.

Message Registers (MRs)
Message registers MR0 through MR7 map to the local registers of the current window in the processor’s general purpose register file for IPC and LIPC calls, otherwise they are located in the UTCB. The remaining message registers map to memory locations in the UTCB. MR0 starts at byte offset 512 in the UTCB, and successive message registers follow in memory.
VIRTUAL REGISTERS

Buffer Registers (BRs)
The buffer registers map to memory locations in the UTCB. BR₀ is at byte offset 248 in the UTCB, BR₁ at byte offset 256, etc.

UTCB Memory With Undefined Semantics
The kernel will associate no semantics with memory located at \( \text{UTCB address} + 80 \ldots \text{UTCB address} + 247 \). The application can use this memory as thread local storage, e.g., for implementing the L4 API. Note, however, that the memory contents within this region may be overwritten during a system-call operating on message registers.

All undefined UTCB memory which is not covered by the above mentioned region may have kernel defined semantics.
G.2 Systemcalls [SPARC-v9]

The system-calls which are invoked by the jmpl instruction take the target of the calls from the system call link fields in the kernel interface page (see page 2). Each system-call link value specifies an address relative to the kernel interface page’s base address. One may invoke the system calls with any instruction that branches to the appropriate target, as long as the return-address is contained in $o7$.

The locations of the system-calls are fixed during the life of an application, although they may change outside of the life of an application. It is not valid to prelink an application against a set of system call locations. The official locations are always provided in the KIP.

The system call definitions below only specify the contexts of the general purpose registers. Except for the KERNELINTERFACE system-call, the contents of user accessible state registers are assumed to be scratched. The floating-point registers are assumed to be preserved across system calls.

---

**KERNELINTERFACE** [Slow Systemcall]

$$
\begin{array}{l}
- \quad g0 \ldots g7 \\
- \quad o0 \\
- \quad o1 \\
- \quad o2 \\
- \quad o3 \\
- \quad o4, o5 \\
- \quad o6, o7 \\
- \quad l0 \ldots l7 \\
- \quad l0 \ldots l7 \\
\end{array}
\rightarrow
\begin{array}{l}
- \quad g0 \ldots g7 \\
- \quad o0 \\
- \quad o1 \\
- \quad o2 \\
- \quad o3 \\
- \quad o4, o5 \\
- \quad o6, o7 \\
- \quad l0 \ldots l7 \\
- \quad l0 \ldots l7 \\
\end{array}
$$

For this system-call, all registers other than the output registers are preserved.

---

**EXCHANGEREGISTERS** [Systemcall]

$$
\begin{array}{l}
- \quad g0 \ldots g7 \\
- \quad dest \\
- \quad control \\
- \quad SP \\
- \quad IP \\
- \quad pager \\
- \quad UserDefinedHandle \\
- \quad FLAGS \\
- \quad o0 \\
- \quad o1 \\
- \quad o2 \\
- \quad o3 \\
- \quad o4 \\
- \quad o5 \\
- \quad o6, o7 \\
- \quad l0 \ldots l7 \\
- \quad l0 \ldots l7 \\
\end{array}
\rightarrow
\begin{array}{l}
- \quad g0 \ldots g7 \\
- \quad o0 \\
- \quad o1 \\
- \quad o2 \\
- \quad o3 \\
- \quad o4 \\
- \quad o5 \\
- \quad o6, o7 \\
- \quad l0 \ldots l7 \\
- \quad l0 \ldots l7 \\
\end{array}
$$

Notes: FLAGS might simply be set from the current values of the caller. Think about this some more...

---

**THREADCONTROL** [Privileged Systemcall]

$$
\begin{array}{l}
- \quad g0 \ldots g7 \\
- \quad dest \\
- \quad space \\
- \quad scheduler \\
- \quad pager \\
- \quad UtcLocation \\
- \quad o0 \\
- \quad o1 \\
- \quad o2 \\
- \quad o3 \\
- \quad o4 \\
- \quad o5 \\
- \quad o6, o7 \\
- \quad l0 \ldots l7 \\
- \quad l0 \ldots l7 \\
\end{array}
\rightarrow
\begin{array}{l}
- \quad g0 \ldots g7 \\
- \quad o0 \\
- \quad o1 \\
- \quad o2 \\
- \quad o3 \\
- \quad o4 \\
- \quad o5 \\
- \quad o6, o7 \\
- \quad l0 \ldots l7 \\
- \quad l0 \ldots l7 \\
\end{array}
$$

Notes: It is only valid to prelink an application against a set of system call locations if the locations are fixed during the life of an application.
### SystemClock [Systemcall]

- `g0...g7`
- `o0`
- `o1...o5`
- `o6, o7`
- `i0...i7`
- `i0...i7` → SystemClock

- `g0...g7` → `g0...g7`
- `o0` → `clock`
- `o1...o5` → `~`
- `o6, o7` → `~`
- `i0...i7` → `~`
- `i0...i7` → `~`

### ThreadSwitch [Systemcall]

- `g0...g7`
- `dest` `o0`
- `o1...o5`
- `o6, o7`
- `i0...i7`
- `i0...i7` → ThreadSwitch

- `g0...g7` → `g0...g7`
- `o0` → `~`
- `o1...o5` → `~`
- `o6, o7` → `~`
- `i0...i7` → `~`
- `i0...i7` → `~`

### Schedule [Systemcall]

- `g0...g7`
- `dest` `o0`
- `time control` `o1`
- `processor control` `o2`
- `priority` `o3`
- `preemption control` `o4`
- `o5`
- `o6, o7`
- `i0...i7`
- `i0...i7` → Schedule

- `g0...g7` → `g0...g7`
- `o0` → `result`
- `o1` → `time control`
- `o2` → `~`
- `o3` → `~`
- `o4` → `~`
- `o5` → `~`
- `o6, o7` → `~`
- `i0...i7` → `~`
- `i0...i7` → `~`

### IPC [Systemcall]

- `g0...g6`
- `UTCB` `o7`
- `FromSpecifier` `o0`
- `to` `o1`
- `Timeouts` `o2`
- `o3...o5`
- `o6, o7`
- `MR0` `i0`
- `MR1` `i1`
- `MR2` `i2`
- `MR3` `i3`
- `MR4` `i4`
- `MR5` `i5`
- `MR6` `i6`
- `MR7` `i7`
- `i0...i5`
- `i6, i7` → Ipc

- `g0...g6` → `~`
- `o7` → `~`
- `o0` → `from`
- `o1` → `~`
- `o2` → `~`
- `o3...o5` → `~`
- `o6, o7` → `~`
- `i0` → `MR0`
- `i1` → `MR1`
- `i2` → `MR2`
- `i3` → `MR3`
- `i4` → `MR4`
- `i5` → `MR5`
- `i6` → `MR6`
- `i7` → `MR7`
- `i0...i5` → `~`
- `i6, i7` → `~`
**IPC** [Systemcall]

<table>
<thead>
<tr>
<th>UTCB</th>
<th>FromSpecifier</th>
<th>Timeouts</th>
<th>MR</th>
<th>MR</th>
<th>MR</th>
<th>MR</th>
<th>MR</th>
<th>MR</th>
<th>–</th>
<th>–</th>
</tr>
</thead>
<tbody>
<tr>
<td>g8</td>
<td>o0</td>
<td>a2</td>
<td>10</td>
<td>11</td>
<td>12</td>
<td>13</td>
<td>14</td>
<td>15</td>
<td>16</td>
<td>17</td>
</tr>
<tr>
<td>g0...g6</td>
<td>from</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Lipc** →

| – | – | – | – | – | – | – | – | – | – | – |
| g0...g6 | ~ | g7 | = | o0 | from | o1 | ~ | o2 | ~ | o3...o5 | ~ | o6, o7 | = | o4...o8 | ~ | o9...o15 | ~ | o16, o17 | ~ |

**Unmap** [Systemcall]

| Unmap | – | – | – | – | – | – | – | – | – | – |
| g0...g7 | ~ | g0 | = | o1...o5 | ~ | o6, o7 | = | i0...i17 | ~ | i0...i17 | ~ | l0...l17 | ~ |

**SpaceControl** [Privileged Systemcall]

| SpaceControl | – | – | – | – | – | – | – | – | – | – |
| g0...g7 | ~ | g0 | = | o1 | control | o2 | ~ | o3 | ~ | o4 | ~ | o5 | ~ | o6, o7 | ~ | i0...i17 | ~ | i0...i17 | ~ |

**ProcessorControl** [Privileged Systemcall]

<p>| ProcessorControl | – | – | – | – | – | – | – | – | – | – |
| g0...g7 | ~ | g0 | = | o1 | result | o2 | ~ | o3 | ~ | o4 | ~ | o5 | ~ | o6, o7 | ~ | i0...i17 | ~ | i0...i17 | ~ |</p>
<table>
<thead>
<tr>
<th>control</th>
<th>$o_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>attribute$_0$</td>
<td>$o_1$</td>
</tr>
<tr>
<td>attribute$_1$</td>
<td>$o_2$</td>
</tr>
<tr>
<td>attribute$_2$</td>
<td>$o_3$</td>
</tr>
<tr>
<td>attribute$_3$</td>
<td>$o_4$</td>
</tr>
<tr>
<td>$\sim$</td>
<td>$o_5$</td>
</tr>
<tr>
<td>$\sim$</td>
<td>$o_6, o_7$</td>
</tr>
<tr>
<td>$\sim$</td>
<td>$i_0 \ldots i_7$</td>
</tr>
<tr>
<td>$\equiv$</td>
<td>$l_0 \ldots l_7$</td>
</tr>
<tr>
<td>$\equiv$</td>
<td>$i_0 \ldots i_7$</td>
</tr>
</tbody>
</table>

- **Memory Control** →

  $\text{jmpl MemoryControl}$

  | $\sim$ | $o_0$ |
  | $\sim$ | $o_1$ |
  | $\sim$ | $o_2$ |
  | $\sim$ | $o_3$ |
  | $\sim$ | $o_4$ |
  | $\equiv$ | $o_5$ |
  | $\equiv$ | $o_6, o_7$ |
  | $\equiv$ | $i_0 \ldots i_7$ |
  | $\equiv$ | $i_0 \ldots i_7$ |
G.3 Memory Attributes [SPARC v9]

TODO!
G.4 Exception Message Format [SPARC v9]

TODO!
G.5 Booting [SPARC v9]

TODO!
These remarks illuminate the design process from version 2 to version 4.

H.1 Exception Handling

The current model decided upon for exception handling in L4 is to associate an exception handler thread with each thread in the system (see page 66). This model was chosen because it allowed us to handle exceptions generically without introducing any new concepts into the API. It also closely resembles the current page fault handling model.

Another model for exception handling is to use callbacks. Using this model an instruction pointer for a callback function and a pointer to an exception state save area is associated with each thread. Upon catching an exception the kernel stores the cause of the exception into the save area and transfers execution to the exception callback function.

It is evident that the callback model can be faster than the IPC model because the callback model may require only one control transfer into the kernel whereas the IPC model will require at least two. Nevertheless, the IPC model was chosen because it introduces no new mechanisms into the kernel, and we are currently not aware of any real life scenario where the extra performance gain you very much. There exists a challenge to prove these claims wrong. See http://l4hq.org/fun/ for the rules of the challenge.
## Table of Procs, Types, and Constants

| ! (CacheAllocationHint l, r) bool | none | 54 |
| ! (Clock l, r) bool | none | 26 |
| ! (MsgTag l, r) bool | none | 46 |
| ! (ThreadId l, r) bool | none | 15 |
| ! (Time l, r) bool | none | 29 |
| + (Acceptor l, r) Acceptor | none | 55 |
| + (Clock l, int r) Clock | none | 26 |
| + (Clock l, Word64 r) Clock | none | 26 |
| + (Fpage f, Word AccessRights) Fpage | none | 37 |
| + (MsgTag t, Word label) MsgTag | none | 46 |
| + (StringItem s, CacheAllocationHint h) StringItem | none | 54 |
| + (Time l, r) Time | none | 29 |
| + (Time l, Word r) Time | none | 29 |
| + = (Acceptor l, r) Acceptor | none | 55 |
| + = (Fpage f, Word AccessRights) Fpage | none | 37 |
| + = (MsgTag t, Word label) MsgTag | none | 46 |
| + = (StringItem& dest, StringItem AdditionalSubstring) StringItem & | none | 53 |
| + = (StringItem& dest, Void* AdditionalSubstringAddress) StringItem & | none | 53 |
| + = (StringItem s, CacheAllocationHint h) StringItem | none | 54 |
| + = (Time l, r) Time | none | 29 |
| + = (Time l, Word r) Time | none | 29 |
| - (Acceptor l, r) Acceptor | none | 55 |
| - (Clock l, int r) Clock | none | 26 |
| - (Clock l, Word64 r) Clock | none | 26 |
| - (Fpage f, Word AccessRights) Fpage | none | 37 |
| - (Time l, r) Time | none | 29 |
| - (Time l, Word r) Time | none | 29 |
| - = (Acceptor l, r) Acceptor | none | 55 |
| - = (Fpage f, Word AccessRights) Fpage | none | 37 |
| - = (Time l, r) Time | none | 29 |
| < (Clock l, r) bool | none | 26 |
| < (Time l, r) bool | none | 29 |
| <= (Clock l, r) bool | none | 26 |
| <= (Time l, r) bool | none | 29 |
| == (CacheAllocationHint l, r) bool | none | 54 |
| == (Clock l, r) bool | none | 26 |
| == (MsgTag l, r) bool | none | 46 |
| == (ThreadId l, r) bool | none | 15 |
| == (Time l, r) bool | none | 29 |
| > (Clock l, r) bool | none | 26 |
| > (Time l, r) bool | none | 29 |
| >= (Clock l, r) bool | none | 26 |
| >= (Time l, r) bool | none | 29 |

\textbf{AbortIpc and stop} (ThreadId t) ThreadState \hspace{1em} \textbf{ExchangeRegisters} 21
\textbf{AbortIpc and stop} (ThreadId t, Word& sp, ip, flags) ThreadState \hspace{1em} \textbf{ExchangeRegisters} 21
\textbf{AbortReceive and stop} (ThreadId t) ThreadState \hspace{1em} \textbf{ExchangeRegisters} 21
\textbf{AbortReceive and stop} (ThreadId t, Word& sp, ip, flags) ThreadState \hspace{1em} \textbf{ExchangeRegisters} 21
\textbf{AbortSend and stop} (ThreadId t) ThreadState \hspace{1em} \textbf{ExchangeRegisters} 21
<table>
<thead>
<tr>
<th>Procedure</th>
<th>Documentation</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>AbortSend_and_stop</td>
<td>(ThreadId t, Word&amp; sp, ip, flags) ThreadState</td>
<td>EXCHANGEREGISTERS 21</td>
</tr>
<tr>
<td>Accepted</td>
<td>() Acceptor</td>
<td>–none– 56</td>
</tr>
<tr>
<td>Accepted</td>
<td>data type</td>
<td>–n/a– 55</td>
</tr>
<tr>
<td>Accept</td>
<td>(Acceptor a) Void</td>
<td>–none– 56</td>
</tr>
<tr>
<td>Accept</td>
<td>(Acceptor a, MsgBuffer&amp; b) Void</td>
<td>–none– 56</td>
</tr>
<tr>
<td>ACPIMemoryType</td>
<td>Word const</td>
<td>–n/a– 113</td>
</tr>
<tr>
<td>ActualSender</td>
<td>() ThreadId</td>
<td>–none– 17</td>
</tr>
<tr>
<td>ActualSender</td>
<td>() ThreadId</td>
<td>–none– 63</td>
</tr>
<tr>
<td>Address</td>
<td>(Fpage f) Word</td>
<td>–none– 37</td>
</tr>
<tr>
<td>AllocateNewCacheLines</td>
<td>CacheAllocationHint const</td>
<td>–n/a– 155</td>
</tr>
<tr>
<td>AllocateNewCacheLines</td>
<td>CacheAllocationHint const</td>
<td>–n/a– 95</td>
</tr>
<tr>
<td>AllocateOnlyNewL1CacheLines</td>
<td>CacheAllocationHint const</td>
<td>–n/a– 155</td>
</tr>
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<td>AllocateOnlyNewL1CacheLines</td>
<td>CacheAllocationHint const</td>
<td>–n/a– 95</td>
</tr>
<tr>
<td>anylocalthread</td>
<td>ThreadId const</td>
<td>–n/a– 15</td>
</tr>
<tr>
<td>anythread</td>
<td>ThreadId const</td>
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</tr>
<tr>
<td>ApiFlags</td>
<td>() Word</td>
<td>–none– 8</td>
</tr>
<tr>
<td>ApiVersion</td>
<td>() Word</td>
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<td>Append</td>
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<td>–none– 56</td>
</tr>
<tr>
<td>Append</td>
<td>(MsgBuffer&amp; b, StringItem s) Void</td>
<td>–none– 56</td>
</tr>
<tr>
<td>Append</td>
<td>(Msg&amp; msg, GrantItem g) Void</td>
<td>–none– 47</td>
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<tr>
<td>Append</td>
<td>(Msg&amp; msg, MapItem m) Void</td>
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<td>(Msg&amp; msg, StringItem s) Void</td>
<td>–none– 47</td>
</tr>
<tr>
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<td>(Msg&amp; msg, StringItem&amp; s) Void</td>
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<td>ArchitectureSpecificMemoryType</td>
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</tr>
<tr>
<td>AssociateInterrupt</td>
<td>(ThreadId InterruptThread, InterruptHandler) Word</td>
<td>–none– 24</td>
</tr>
<tr>
<td>BootInfo</td>
<td>(Void* KernelInterface) Word</td>
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</tr>
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<td>BootLoaderSpecificMemoryType</td>
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<td>(StringItem s) CacheAllocationHint</td>
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<td>CacheAllocationHint</td>
<td>data type</td>
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<td>CacheAllocationHint const</td>
<td>–n/a– 111</td>
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<td>CacheNonTemporalL1</td>
<td>CacheAllocationHint const</td>
<td>–n/a– 111</td>
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<td>CacheNonTemporalL2</td>
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<td>Word const</td>
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</tr>
<tr>
<td>CachingInhibitedMemory</td>
<td>Word const</td>
<td>–n/a– 122</td>
</tr>
<tr>
<td>Call</td>
<td>(ThreadId to) MsgTag</td>
<td>IPC 61</td>
</tr>
<tr>
<td>Call</td>
<td>(ThreadId to, Time SndTimeout, RcvTimeout) MsgTag</td>
<td>IPC 62</td>
</tr>
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<td>Clear</td>
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<td>Clr_CopFlag</td>
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</tr>
<tr>
<td>CompleteAddressSpace</td>
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<td>DisablePreemptionFaultException</td>
<td>() bool</td>
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</tr>
<tr>
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<td>() bool</td>
<td>–none– 34</td>
</tr>
<tr>
<td>DoNotAllocateNewCacheLines</td>
<td>CacheAllocationHint const</td>
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</tr>
<tr>
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</tr>
<tr>
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<tr>
<td>ErrorCode</td>
<td>() Word</td>
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<td>ExceptionHandler</td>
<td>() ThreadId</td>
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<tr>
<td>ExceptionHandler</td>
<td>() ThreadId</td>
<td>–none– 66</td>
</tr>
<tr>
<td>Procedure/Type/Constant</td>
<td>Description</td>
<td>Page</td>
</tr>
<tr>
<td>--------------------------</td>
<td>-------------</td>
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</tr>
<tr>
<td><code>ExchangeRegisters</code></td>
<td>ThreadId dest, Word control, sp, ip, flags, UserDefinedHandle, ThreadId pager, Word&amp; old_control, old_sp, old_ip, old_flags, old_UserDefinedHandle, ThreadId&amp; old_pager), ThreadId</td>
<td>EXCHANGEREGISTERS 20</td>
</tr>
<tr>
<td><code>eXecutable</code></td>
<td>Word const</td>
<td>n/a-- 37</td>
</tr>
<tr>
<td><code>ExternalFreq</code></td>
<td>(ProcDesc&amp; p) Word</td>
<td>none-- 10</td>
</tr>
<tr>
<td><code>Feature</code></td>
<td>(Void* KernelInterface, Word num) Char*</td>
<td>none-- 9</td>
</tr>
<tr>
<td><code>Flush</code></td>
<td>(Fpage f) Void</td>
<td>UNMAP 40</td>
</tr>
<tr>
<td><code>Flush</code></td>
<td>(Word n, Fpage&amp; [n] fpages) Void</td>
<td>UNMAP 40</td>
</tr>
<tr>
<td><code>FpageLog2</code></td>
<td>(Word BaseAddress, int Log2FpageSize &lt; 64) Fpage</td>
<td>none-- 37</td>
</tr>
<tr>
<td><code>Fpage</code></td>
<td>(Word BaseAddress, int FpageSize ≥ 1K) Fpage</td>
<td>none-- 37</td>
</tr>
<tr>
<td><code>Fpage data type</code></td>
<td>none-- 36</td>
<td></td>
</tr>
<tr>
<td><code>FullyAccessible</code></td>
<td>Word const</td>
<td>none-- 37</td>
</tr>
<tr>
<td><code>GetStatus</code></td>
<td>(Fpage f) Fpage</td>
<td>none-- 40</td>
</tr>
<tr>
<td><code>Get</code></td>
<td>(Msg&amp; msg, Word&amp; ut, {MapItem, GrantItem, StringItem}&amp; Items) Void</td>
<td>none-- 47</td>
</tr>
<tr>
<td><code>GlobalId</code></td>
<td>(ThreadId t) ThreadId</td>
<td>EXCHANGEREGISTERS 15</td>
</tr>
<tr>
<td><code>GlobalId</code></td>
<td>(ThreadId t) ThreadId</td>
<td>EXCHANGEREGISTERS 20</td>
</tr>
<tr>
<td><code>GlobalId</code></td>
<td>(Word threadno, version) ThreadId</td>
<td>none-- 15</td>
</tr>
<tr>
<td><code>GlobalMemory</code></td>
<td>Word const</td>
<td>none-- 122</td>
</tr>
<tr>
<td><code>GrantItem</code></td>
<td>(Fpage f, Word SndBase) GrantItem</td>
<td>none-- 51</td>
</tr>
<tr>
<td><code>GrantItem</code></td>
<td>(GrantItem g) bool</td>
<td>none-- 51</td>
</tr>
<tr>
<td><code>GuardedMemory</code></td>
<td>Word const</td>
<td>none-- 122</td>
</tr>
<tr>
<td><code>High</code></td>
<td>(MemoryDesc&amp; m) Word</td>
<td>none-- 9</td>
</tr>
<tr>
<td><code>IntendedReceiver</code></td>
<td>() ThreadId</td>
<td>none-- 17</td>
</tr>
<tr>
<td><code>IpcFailed</code></td>
<td>(Msg Tag t) bool</td>
<td>none-- 62</td>
</tr>
<tr>
<td><code>IpcPropagated</code></td>
<td>(Msg Tag t) bool</td>
<td>none-- 62</td>
</tr>
<tr>
<td><code>IpcRedirected</code></td>
<td>(Msg Tag t) bool</td>
<td>none-- 62</td>
</tr>
<tr>
<td><code>IpcSucceeded</code></td>
<td>(Msg Tag t) bool</td>
<td>none-- 62</td>
</tr>
<tr>
<td><code>IpcXcpu</code></td>
<td>(Msg Tag t) bool</td>
<td>none-- 62</td>
</tr>
<tr>
<td><code>Ipc</code></td>
<td>(ThreadId to, FromSpecifier, Word Timeouts, ThreadId&amp; from) MsgTag</td>
<td>IPC 61</td>
</tr>
<tr>
<td><code>IsGlobalId</code></td>
<td>(ThreadId t) bool</td>
<td>none-- 15</td>
</tr>
<tr>
<td><code>IsLocalId</code></td>
<td>(ThreadId t) bool</td>
<td>none-- 15</td>
</tr>
<tr>
<td><code>IsNilFpage</code></td>
<td>(Fpage f) bool</td>
<td>none-- 37</td>
</tr>
<tr>
<td><code>IsNilThread</code></td>
<td>(ThreadId t) bool</td>
<td>none-- 15</td>
</tr>
<tr>
<td><code>IsVirtual</code></td>
<td>(MemoryDesc&amp; m) bool</td>
<td>none-- 9</td>
</tr>
<tr>
<td><code>KernelGenDate</code></td>
<td>(Void* KernelInterface, Word&amp; year, month, day) Void</td>
<td>none-- 8</td>
</tr>
<tr>
<td><code>KernelId</code></td>
<td>() Word</td>
<td>none-- 8</td>
</tr>
<tr>
<td><code>KernelInterface</code></td>
<td>() Void*</td>
<td>KERNELINTERFACE 8</td>
</tr>
<tr>
<td><code>KernelInterface</code></td>
<td>(Word&amp; ApiVersion, ApiFlags, KernelId) Void*</td>
<td>KERNELINTERFACE 8</td>
</tr>
<tr>
<td><code>KernelSupplier</code></td>
<td>(Void* KernelInterface) Word</td>
<td>none-- 8</td>
</tr>
<tr>
<td><code>KernelVersionString</code></td>
<td>(Void* KernelInterface) Char*</td>
<td>none-- 9</td>
</tr>
<tr>
<td><code>KernelVersion</code></td>
<td>(Void* KernelInterface) Word</td>
<td>none-- 8</td>
</tr>
<tr>
<td><code>KipAreaSizeLog2</code></td>
<td>(Void* KernelInterface) Word</td>
<td>none-- 9</td>
</tr>
<tr>
<td><code>Label</code></td>
<td>(Msg &amp; msg) Word</td>
<td>none-- 47</td>
</tr>
<tr>
<td><code>Label</code></td>
<td>(Msg Tag t) Word</td>
<td>none-- 46</td>
</tr>
<tr>
<td><code>LargeSpace</code></td>
<td>Word const</td>
<td>none-- 94</td>
</tr>
<tr>
<td><code>Lcall</code></td>
<td>(ThreadId to) MsgTag</td>
<td>LIPC 62</td>
</tr>
<tr>
<td><code>Lipc</code></td>
<td>(ThreadId to, FromSpecifier, Word Timeouts, ThreadId&amp; from) MsgTag</td>
<td>LIPC 61</td>
</tr>
<tr>
<td><code>LoadBRs</code></td>
<td>(int i, k, Word&amp; k) Void</td>
<td>none-- 11</td>
</tr>
<tr>
<td><code>LoadBRs</code></td>
<td>(int i, Word&amp; k) Void</td>
<td>none-- 56</td>
</tr>
<tr>
<td><code>LoadBR</code></td>
<td>(int i, Word w) Void</td>
<td>none-- 11</td>
</tr>
<tr>
<td><code>LoadBR</code></td>
<td>(int i, Word w) Void</td>
<td>none-- 56</td>
</tr>
<tr>
<td>Name</td>
<td>Type</td>
<td>Page</td>
</tr>
<tr>
<td>----------------------------------------</td>
<td>-------------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td><strong>TABLE OF PROCS, TYPES, AND CONSTANTS</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LoadMRs (int i, k, Word&amp; [k] w) Void</td>
<td>-none-</td>
<td>11</td>
</tr>
<tr>
<td>LoadMRs (int i, k, Word&amp; [k] w) Void</td>
<td>-none-</td>
<td>48</td>
</tr>
<tr>
<td>LoadMR (int i, Word w) Void</td>
<td>-none-</td>
<td>11</td>
</tr>
<tr>
<td>Load (Msg&amp; msg) Void</td>
<td>-none-</td>
<td>48</td>
</tr>
<tr>
<td>LocalId (ThreadId t) ThreadId</td>
<td>EXCHANGEREGISTERS</td>
<td>15</td>
</tr>
<tr>
<td>Load (ThreadId t) ThreadId</td>
<td>EXCHANGEREGISTERS</td>
<td>20</td>
</tr>
<tr>
<td>LocalMemory Word const</td>
<td>-none-</td>
<td>122</td>
</tr>
<tr>
<td>Low (MemoryDesc&amp; m) Word</td>
<td>-none-</td>
<td>9</td>
</tr>
<tr>
<td>LreplyWait (ThreadId to, ThreadId&amp; from) MsgTag</td>
<td>IPC</td>
<td>62</td>
</tr>
<tr>
<td>MapGrantItems (Acceptor a) bool</td>
<td>-none-</td>
<td>56</td>
</tr>
<tr>
<td>MapGrantItems (Fpage RcvWindow) Acceptor</td>
<td>-none-</td>
<td>55</td>
</tr>
<tr>
<td>MapItem (Fpage f, Word SndBase) MapItem</td>
<td>-none-</td>
<td>49</td>
</tr>
<tr>
<td>MapItem (MapItem m) bool</td>
<td>-none-</td>
<td>50</td>
</tr>
<tr>
<td>MapItem data type</td>
<td>-none-</td>
<td>49</td>
</tr>
<tr>
<td>MemoryControl (Word control, Word&amp; attributes[4]) Void</td>
<td>MEMORYCONTROL</td>
<td>70</td>
</tr>
<tr>
<td>MemoryDesc (Void* KernelInterface, Word num) MemoryDesc*</td>
<td>-none-</td>
<td>9</td>
</tr>
<tr>
<td>MemoryDesc data type</td>
<td>-none-</td>
<td>8</td>
</tr>
<tr>
<td>MsgBuffer data type</td>
<td>-none-</td>
<td>56</td>
</tr>
<tr>
<td>MsgTag () MsgTag</td>
<td>-none-</td>
<td>46</td>
</tr>
<tr>
<td>MsgTag (Msg&amp; msg) MsgTag</td>
<td>-none-</td>
<td>47</td>
</tr>
<tr>
<td>MsgTag data type</td>
<td>-none-</td>
<td>46</td>
</tr>
<tr>
<td>Msg data type</td>
<td>-none-</td>
<td>47</td>
</tr>
<tr>
<td>MyGlobalId () ThreadId</td>
<td>-none-</td>
<td>15</td>
</tr>
<tr>
<td>MyGlobalId () ThreadId</td>
<td>-none-</td>
<td>17</td>
</tr>
<tr>
<td>MyLocalId () ThreadId</td>
<td>-none-</td>
<td>15</td>
</tr>
<tr>
<td>MyLocalId () ThreadId</td>
<td>-none-</td>
<td>17</td>
</tr>
<tr>
<td>Myself () ThreadId</td>
<td>-none-</td>
<td>17</td>
</tr>
<tr>
<td>NtPageMemory Word const</td>
<td>-none-</td>
<td>112</td>
</tr>
<tr>
<td>Never Time const</td>
<td>-none-</td>
<td>28</td>
</tr>
<tr>
<td>Nilpage Fpage const</td>
<td>-none-</td>
<td>37</td>
</tr>
<tr>
<td>NilTag MsgTag const</td>
<td>-none-</td>
<td>46</td>
</tr>
<tr>
<td>nilthread ThreadId const</td>
<td>-none-</td>
<td>15</td>
</tr>
<tr>
<td>NoAccess Word const</td>
<td>-none-</td>
<td>37</td>
</tr>
<tr>
<td>NumMemoryDescriptors (Void* KernelInterface) Word</td>
<td>-none-</td>
<td>8</td>
</tr>
<tr>
<td>NumProcessors (Void* KernelInterface) Word</td>
<td>-none-</td>
<td>8</td>
</tr>
<tr>
<td>PageRights (Void* KernelInterface) Word</td>
<td>-none-</td>
<td>8</td>
</tr>
<tr>
<td>Pager () ThreadId</td>
<td>-none-</td>
<td>17</td>
</tr>
<tr>
<td>Pager (ThreadId t) ThreadId</td>
<td>EXCHANGEREGISTERS</td>
<td>20</td>
</tr>
<tr>
<td>PageSizeMask (Void* KernelInterface) Word</td>
<td>-none-</td>
<td>8</td>
</tr>
<tr>
<td>PAL_Call (Word idx, a1, a2, a3, Word&amp; r1, r2, r3) Word</td>
<td>PAL_CALL</td>
<td>104</td>
</tr>
<tr>
<td>PCIConfigFpageLog2 (Word BaseAddress, int Log2FpageSize &lt; 64) Fpage</td>
<td>-none-</td>
<td>110</td>
</tr>
<tr>
<td>PCIConfigFpage (Word BaseAddress, int FpageSize ≥ 256) Fpage</td>
<td>-none-</td>
<td>110</td>
</tr>
<tr>
<td>PreemptionPending () bool</td>
<td>-none-</td>
<td>34</td>
</tr>
<tr>
<td>ProcDesc data type</td>
<td>-none-</td>
<td>8</td>
</tr>
<tr>
<td>ProcessorControl (Word ProcessorNo, control, InternalFrequency, ExternalFrequency, voltage) Word</td>
<td>-none-</td>
<td>69</td>
</tr>
<tr>
<td>ProcessorNo () int</td>
<td>-none-</td>
<td>17</td>
</tr>
<tr>
<td>Put (Msg&amp; msg, Word&amp; [u] ut, int t, [MapItem GrantItem StringItem ]&amp; Items) Void</td>
<td>-none-</td>
<td>47</td>
</tr>
<tr>
<td>Put (Msg&amp; msg, Word&amp; [u] ut, int t, [MapItem GrantItem StringItem ]&amp; Items) Void</td>
<td>-none-</td>
<td>47</td>
</tr>
<tr>
<td>Put (Msg&amp; msg, Word&amp; [u] ut, int t, [MapItem GrantItem StringItem ]&amp; Items) Void</td>
<td>-none-</td>
<td>47</td>
</tr>
<tr>
<td>Put (Msg&amp; msg, Word&amp; [u] ut, int t, [MapItem GrantItem StringItem ]&amp; Items) Void</td>
<td>-none-</td>
<td>47</td>
</tr>
<tr>
<td>Put (Msg&amp; msg, Word&amp; [u] ut, int t, [MapItem GrantItem StringItem ]&amp; Items) Void</td>
<td>-none-</td>
<td>47</td>
</tr>
<tr>
<td>Put (Msg&amp; msg, Word&amp; [u] ut, int t, [MapItem GrantItem StringItem ]&amp; Items) Void</td>
<td>-none-</td>
<td>47</td>
</tr>
<tr>
<td>RecvWindow (Acceptor a) Fpage</td>
<td>-none-</td>
<td>56</td>
</tr>
<tr>
<td>Readable Word const</td>
<td>-none-</td>
<td>36</td>
</tr>
<tr>
<td>ReadExecOnly Word const</td>
<td>-none-</td>
<td>37</td>
</tr>
<tr>
<td>ReadPrecision (Void* KernelInterface) Word</td>
<td>-none-</td>
<td>9</td>
</tr>
<tr>
<td>Receive (ThreadId from) MsgTag</td>
<td>IPC</td>
<td>62</td>
</tr>
<tr>
<td>Receive (ThreadId from, Time RevTimeout) MsgTag</td>
<td>IPC</td>
<td>62</td>
</tr>
</tbody>
</table>
TABLE OF PROCS, TYPES, AND CONSTANTS

<table>
<thead>
<tr>
<th>Procedure/Type/Constant</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ReplyWait</td>
<td>(Threadid t, from) MsgTag</td>
<td>IPC</td>
</tr>
<tr>
<td>ReplyWait</td>
<td>(Threadid t, from RcVTimeout, Threadid &amp; from) MsgTag</td>
<td>IPC</td>
</tr>
<tr>
<td>Reply</td>
<td>(Threadid t) MsgTag</td>
<td>IPC</td>
</tr>
<tr>
<td>ReservedMemoryType</td>
<td>Word const</td>
<td>--un--</td>
</tr>
<tr>
<td>Rights</td>
<td>(Fpage f) Word</td>
<td>--none--</td>
</tr>
<tr>
<td>SAL_Call</td>
<td>(Word idx, a1, a2, a3, a4, a5, a6, Word &amp; r1, r2, r3) Word</td>
<td>SAL_CALL</td>
</tr>
<tr>
<td>SAL_PCI_ConfigRead</td>
<td>(Word address, size, Word &amp; value) Word</td>
<td>SAL_CALL</td>
</tr>
<tr>
<td>SAL_PCI_ConfigWrite</td>
<td>(Word address, size, value) Word</td>
<td>SAL_CALL</td>
</tr>
<tr>
<td>SameThreads</td>
<td>(Threadid t, r) bool</td>
<td>EXCHANGE_REGISTER</td>
</tr>
<tr>
<td>SchedulePrecision</td>
<td>(Void * KernelInterface) Word</td>
<td>--none--</td>
</tr>
<tr>
<td>Schedule</td>
<td>(Threadid dest, Word TimeControl, ProcessorControl, prio, PreemptionControl, &amp; old_TimeControl) Word</td>
<td>SCHEDULE</td>
</tr>
<tr>
<td>Send</td>
<td>(Threadid t) MsgTag</td>
<td>IPC</td>
</tr>
<tr>
<td>Send</td>
<td>(Threadid t, Time SndTimeout) MsgTag</td>
<td>IPC</td>
</tr>
<tr>
<td>Set_CopFlag</td>
<td>(Word n) Void</td>
<td>--none--</td>
</tr>
<tr>
<td>Set_CopFlag</td>
<td>(Word n) Void</td>
<td>--none--</td>
</tr>
<tr>
<td>Set_ExceptionHandler</td>
<td>(Threadid new) Void</td>
<td>--none--</td>
</tr>
<tr>
<td>Set_ExceptionHandler</td>
<td>(Threadid NewHandler) Void</td>
<td>--none--</td>
</tr>
<tr>
<td>Set_Label</td>
<td>(Msg &amp; msg) Word label</td>
<td>--none--</td>
</tr>
<tr>
<td>Set_MsgTag</td>
<td>(MsgTag t) Void</td>
<td>--none--</td>
</tr>
<tr>
<td>Set_MsgTag</td>
<td>(Msg &amp; msg) MsgTag t Void</td>
<td>--none--</td>
</tr>
<tr>
<td>Set_PageAttribute</td>
<td>(Fpage f, Word attribute) Void</td>
<td>MEMORY_CONTROL</td>
</tr>
<tr>
<td>Set_Pager</td>
<td>(Threadid NewPager) Void</td>
<td>--none--</td>
</tr>
<tr>
<td>Set_Pager</td>
<td>(Threadid t, p) Void</td>
<td>EXCHANGE_REGISTER</td>
</tr>
<tr>
<td>Set_PreemptionDelay</td>
<td>(Threadid dest, Word sensitivePrio, Word maxDelay) Word</td>
<td>--none--</td>
</tr>
<tr>
<td>Set_Priority</td>
<td>(Threadid dest, Word prio) Word</td>
<td>--none--</td>
</tr>
<tr>
<td>Set_ProcessorNo</td>
<td>(Threadid dest, Word ProcessorNo) Word</td>
<td>--none--</td>
</tr>
<tr>
<td>Set_Propagation</td>
<td>(Msg &amp; Tag t) Void</td>
<td>--none--</td>
</tr>
<tr>
<td>Set_Rights</td>
<td>(Fpage f, Word AccessRights) Void</td>
<td>--none--</td>
</tr>
<tr>
<td>Set_Timeslice</td>
<td>(Threadid dest, Time ts, Time tq) Word</td>
<td>--none--</td>
</tr>
<tr>
<td>Set_UserDefinedHandler</td>
<td>(Threadid t, Word handle) Void</td>
<td>EXCHANGE_REGISTER</td>
</tr>
<tr>
<td>Set_UserDefinedHandler</td>
<td>(Word NewValue) Void</td>
<td>--none--</td>
</tr>
<tr>
<td>Set_VirtualSender</td>
<td>(Threadid t) Void</td>
<td>--none--</td>
</tr>
<tr>
<td>Set_VirtualSender</td>
<td>(Threadid t) Void</td>
<td>--none--</td>
</tr>
<tr>
<td>Set_XferTimeouts</td>
<td>(Word NewValue) Void</td>
<td>--none--</td>
</tr>
<tr>
<td>SharedMemoryType</td>
<td>Word const</td>
<td>--none--</td>
</tr>
<tr>
<td>SizeLog2</td>
<td>(Fpage f) Word</td>
<td>--none--</td>
</tr>
<tr>
<td>Size</td>
<td>(Fpage f) Word</td>
<td>--none--</td>
</tr>
<tr>
<td>Sleep</td>
<td>(Time t) Void</td>
<td>IPC</td>
</tr>
<tr>
<td>SmallSpace</td>
<td>(Word location, size) Word</td>
<td>--none--</td>
</tr>
<tr>
<td>SndBase</td>
<td>(Granitem g) Word</td>
<td>--none--</td>
</tr>
<tr>
<td>SndBase</td>
<td>(MapItem m) Word</td>
<td>--none--</td>
</tr>
<tr>
<td>SndFpage</td>
<td>(Granitem g) Fpage</td>
<td>--none--</td>
</tr>
<tr>
<td>SndFpage</td>
<td>(MapItem m) Fpage</td>
<td>--none--</td>
</tr>
<tr>
<td>SpaceControl</td>
<td>(Threadid, SpaceSpecifier, Word control, Fpage KernelInterface, FacePageArea, UtcbArea, ThreadId Redirector, Word &amp; old_Control) Word</td>
<td>SPACE_CONTROL</td>
</tr>
<tr>
<td>SpeculativeMemory</td>
<td>Word const</td>
<td>--none--</td>
</tr>
<tr>
<td>Start</td>
<td>(Threadid t) Void</td>
<td>EXCHANGE_REGISTER</td>
</tr>
<tr>
<td>Start</td>
<td>(Threadid t, Word sp, ip) Void</td>
<td>EXCHANGE_REGISTER</td>
</tr>
<tr>
<td>Start</td>
<td>(Threadid t, Word sp, ip, flags) Void</td>
<td>EXCHANGE_REGISTER</td>
</tr>
<tr>
<td>Stop</td>
<td>(Threadid t) ThreadState</td>
<td>EXCHANGE_REGISTER</td>
</tr>
<tr>
<td>Stop</td>
<td>(Threadid t, Word &amp; sp, ip, flags) ThreadState</td>
<td>EXCHANGE_REGISTER</td>
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<td><code>SystemClock</code> () Clock</td>
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<td><code>ThreadControl</code> (ThreadId dest, SpaceSpecifier, Scheduler, Pager, Void* Utclo- cation) Word</td>
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<td>Procs/TYPES/CONSTANTS</td>
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<td><strong>Yield</strong> () Void</td>
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<td><strong>ZeroTime</strong> Time const</td>
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Index

!=, 15, 26, 29
+, 26, 29, 37, 46, 54, 55
+=, 26, 29, 37, 46, 53–55
−, 26, 29, 37, 55
− (ignored), vii
=, 29, 37, 55
<, 26, 29
<=, 26, 29
≡ (unchanged), vii
== , 15, 26, 29, 46, 54
>, 26, 29
>=, 26, 29
∼ (undefined), vii

σo, see sigma0

AbortIpce_and_stop, 21
AbortReceive_and_stop, 21
AbortSend_and_stop, 21
Accept, 56
Accepted, 56
acceptor, 55
ACPIMemoryType, 113
ActualSender, 17, 63
Address, 37
address space
    creation/deletion, 41
    initial, 79
AllocateNewCacheLines, 95, 155
AllocateOnlyNewL1CacheLines, 95, 155
anylocalthread, 15
anythread, 15
ApiFlags, 8
ApiVersion, 8
Append, 47, 56
ArchitectureSpecificMemoryType, 9
AssociateInterrupt, 24

BootInfo, 9
booting, 82–84
    alpha, 134
    amd64, 159
    ia32, 99
    mips64, 144
    powerpc, 126
    sparc64, 170
BootLoaderSpecificMemoryType, 9
BR, see buffer registers
buffer registers, 55
    alpha, 129
    amd64, 147–148
    ia32, 87–88
    ia64, 103
    mips64, 137, 163
    powerpc, 117
    sparc64, 163

cacheability, 52, 95, 96, 111, 112, 122, 143, 155, 156, 168
CacheAllocationHint, 54
CacheNonTemporalAllLevels, 111
CacheNonTemporalL1, 111
CacheNonTemporalL2, 111
CachingEnabledMemory, 122
CachingInhibitedMemory, 122
Call, 61, 62
Clear, 47, 56
clock, 26
    reading, 27
Clr_CopFlag, 17, 67
CompleteAddressSpace, 37
ComparseString, 53
convenience programming interface, vi
ConventionalMemoryType, 9
coprocessors, 67
DeassociateInterrupt, 24
debug registers, 98, 158
DedicatedMemoryType, 9
DefaultMemory, 70, 96, 112, 122, 156
DisablePreemption, 34
DisablePreemptionFaultException, 34
DoNotAllocateNewCacheLines, 95, 155

EnablePreemption, 34
EnablePreemptionFaultException, 34
endian, 3
ErrorCode, 17, 62
exception
    handling, 66
    message
        amd64, 157
        ia32, 97
        ia64, 114
        powerpc, 123
        sparc64, 169
protocol, 78
ExceptionHandler, 17, 66
ExchangeRegisters, 20
eXecutable, 37
ExternalFreq, 10

Feature, 9
Flash, 40
Fpage, 37
fpage, 36–37
    mapping, 57
    receiving, 55
unmapping, 36, 38–40
FpageLog2, 37
FullyAccessible, 37

generic binary interface, vi
generic programming interface, vi
Get, 47, 48
GetStatus, 40
global thread ID, 14
GlobalId, 15, 20
GlobalMemory, 122
GrantItem, 51
GuardedMemory, 122
High, 9
include files, viii
IntendedReceiver, 17, 62
InternalFreq, 10
interrupt
association, 22
thread ID, 14
IO fpage, 93, 154
IoFpage, 93, 154
IoFpageLog2, 93, 154
IPC, 57–63
aborting, 18
cross cpu, 60
propagation, 58
Ipc, 61
IpcFailed, 62
IpcRedirected, 62
IpcSucceeded, 62
IpcXcpu, 62
IsGlobalId, 15
IsLocalId, 15
IsNilFpage, 37
IsNilThread, 15
IsVirtual, 9
kernel features, 5
ia32, 92
kernel interface page, 2–10
data structure, 2–6
location, 41
retrieving, 7–10
KernelGenDate, 8
KernelId, 8
KernelInterface, 8
KernelSupplier, 8
KernelVersion, 8
KernelVersionString, 9
KipAreaSizeLog2, 9
Label, 46, 47
LargeSpace, 94
Leall, 62
Lipc, 61
lipc, 57
Load, 47
LoadBR, 11, 56
LoadBrs, 11, 56
LoadMR, 11, 48
LoadMRs, 11, 48
local ipc, 57
local thread ID, 14
LocalId, 15, 20
LocalMemory, 122
logical interface, vi
Low, 9
LreplyWait, 62
MapGrantItems, 55, 56
MapItem, 49, 50
memory descriptor, 6, 83–84
ia64, 113
MemoryControl, 70
MemoryDesc, 9
message registers, 44–45
alpha, 128–129
amd64, 146–147
ia32, 87
ia64, 102–103
mips64, 136–137
powerpc, 116–117
sparc64, 162–163
messages
generating, 44–48
model specific registers, 98, 158
MR, see message registers
MsgTag, 46, 47
MyGlobalId, 15, 17
MyLocalId, 15, 17
Myself, 15, 17
NaTPageMemory, 112
Never, 28
Nilpage, 37
Niltag, 46
nilthread, 15
NoAccess, 37
NumMemoryDescriptors, 8
NumProcessors, 8
page
access rights, 4, 36, 49, 51, 76, 80
changing, 38, 49, 51
inspecting, 39
attributes, 80
amd64, 156
ia32, 96
ia64, 112
mips64, 143
powerpc, 122
sparc64, 168
size, 3
pagefault
protocol, 76
Pager, 17, 20
pager, 76
changing, 17, 20, 23
PageRights, 8
PageSizeMask, 8
PAL procedure calls, 104
PAL_Call, 104
PCI Config fpage, 110
PCI Configuration Space
ia64, 104, 110
PCIconfigFpage, 110
PCIconfigFpageLog2, 110
preemption, 31, 34
protocol, 77
PreemptionPending, 34
privileged threads, vii
ProcDesc, 9
processor-specific binary interface, vi
ProcessorControl, 69
ProcessorNo, 16
ProcessorNo, 17
propagation, 58
Put, 47, 48
RcvWindow, 56
RDMSR, 98, 158
Readable, 36
ReadExecOnly, 37
ReadPrecision, 9
Receive, 62
redirection, 42, 58
Reply, 62
ReplyWait, 62
ReservedMemoryType, 9
Rights, 37
SAL procedure calls, 104
SAL_Call, 104
SAL_PCI_ConfigRead, 104
SAL_PCI_ConfigWrite, 104
SameThreads, 15
Schedule, 33
SchedulePrecision, 9
segments, 98, 158
Send, 62
send base, 49
sensitive prio, 31
Set_CopFlag, 17, 67
Set_ExceptionHandler, 17, 66
Set_Label, 47
Set_MsgTag, 46, 47
Set_PageAttribute, 71
Set_Pager, 17, 20
Set_PagesAttributes, 71
Set_PreemptionDelay, 33
Set_Priority, 33
Set_ProcessorNo, 33
Set_Propagation, 63
Set_Rights, 37
Set_Timeslice, 33
Set_UserDefinedHandle, 17, 20
Set_VirtualSender, 17, 63
Set_XferTimeouts, 17
SharedMemoryType, 9
sigma0, 79
protocol, 79–81
Size, 37
SizeLog2, 37
Sleep, 62
small spaces, 94
SmallSpace, 94
SndBase, 50, 51
SndPage, 50, 51
SpaceControl, 42
SpeculativeMemory, 122
Start, 20
Stop, 21
Store, 47
StoreBR, 11, 56
StoreBRS, 11, 56
StoreMR, 11, 48
StoreMRs, 11, 48
Stringhem, 53
Stringhems, 56
StringhemsAcceptor, 55
strings, 52–54
receiving, 55
Substring, 53
Substrings, 53
system thread, 14, 62
system-call links, 5
alpha, 130–133
amd64, 149
ia32, 89
ia64, 105
mips64, 138–142
powerpc, 118–121
sparc64, 164
SystemBase, 4
SystemClock, 27
TCR, see thread control registers
thread creation, 22
halting, 18
ID, 14
id, 15, see thread ID
migration, 32
priority, 31
privileged, vii
startup protocol, 74
state, 21, 32
version, 14, 22
thread control registers, 16–17
alpha, 128
amd64, 146
ia32, 86
ia64, 102
mips64, 136
powerpc, 116
sparc64, 162
thread ID, 14–15
retrieving, 17, 20
ThreadControl, 23
ThreadIdBits, 8
ThreadIdSystemBase, 8
ThreadIdUserBase, 9
ThreadNo, 15
ThreadSwitch, 30
ThreadWasHalted, 21
ThreadWasIpcing, 21
ThreadWasReceiving, 21
ThreadWasSending, 21
time, 28–29
time quantum, 31
Timeouts, 63
TimePeriod, 28
TimePoint, 29
timeslice, 31
donation, 30
Type, 9
TypedWords, 46
UncacheableExportedMemory, 112
UncacheableMemory, 96, 112, 156
UndefinedMemoryType, 9
Unmap, 39
UntypedWords, 46
UntypedWordsAcceptor, 55
upward compatibility, vii
UseDefaultCacheLineAllocation, 53, 95, 111, 155
UserBase, 4
UserDefinedHandle, 16, 19
UserDefinedHandle, 17, 20
using the API, viii
UTCB
  location, 41
  size, 4, 23, 41
UtcbAlignmentLog2, 9
UtcbAreaSizeLog2, 9
UtcbSize, 9

Version, 15
virtual registers, 11

Wait, 62
WasExecuted, 40
WasReferenced, 40
WasWritten, 40
Word, vii
Word16, vii
Word32, vii
Word64, vii
Writable, 36
WriteBackMemory, 96, 112, 122, 156
WriteCoalescingMemory, 112
WriteCombiningMemory, 96, 156
WriteProtectedMemory, 96, 156
WriteThroughMemory, 96, 122, 156
WRMSR, 98, 158

XferTimeouts, 17

Yield, 30

ZeroTime, 28